CMV Reference Manual

ADSL Software Specification

Revision History

Manual Revision Number 1.0
Issued January 22, 2002
Documentation Number 0014

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CMV Formats

This chapter describes the Configuration and Management Variables in reference format.

The programmer needs to be concerned about the system in which the data link is embedded as a whole. The programmable interfaces will be located in the ME-C and the ME-R. To program the ATU-C or the ATU-R may require breaking the data path by taking the ATUs offline.

Chapter 2 details the message interface that the ME can use to transport CMV names and data values over the MP control path. A message carries the value in the Memory Access Data Field, which is 32 bits long. The bit-maps in this chapter map the fields and flags of the CMV values to the bits of these datawords.

There is not necessarily a coincidence of nibble or byte boundaries with field boundaries. A 4-bit field might straddle two nibbles. Nevertheless, the field values are stated here as though the field were an integral whole. For example, **0x1** would be represented as a value of **0001** for a 4-bit field, even though the low-order **01** and the high-order **00** might fall into different nibbles.

The message sends a complete dataword of 8 nibbles, each represented by one hexadecimal digit. In **0x5A001321** (a fictional dataword), a given field probably straddles at least two of these digits. You can find some examples of datawords and the field values transported by them in Chapter 4.

Some CMV values require more than one dataword. One message, however, contains only one dataword. In those cases, the ME sends a sequence of **n** messages to transport **n** datawords.

By convention, the base address plus the offset is the name of the variable. In the “Summary” tables of this chapter, multiple offsets may be listed next to the CMV name, up to the number of datawords required.

In some cases it is convenient to state a symbolic name for each of a sequence of datawords. The names do not necessarily reference contiguous datawords. Some of the intervening datawords may not be named.

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For example, in places you will see a name such as TXDA.(reserved) at offset 0. This notation means that the dataword at the location TXDA + 0 has no symbolic name and is reserved.

This manual generally details datawords only where necessary to describe the fields and bits within them. It is not necessary to provide a bit chart when the value takes up the entire 32 bits, or when the dataword is reserved. Similarly, in tables of values, only values of valid fields and bits appear. Reserved bits are shaded.

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CMV Quick View

Table 1 gives you a quick view of the CMVs detailed in this chapter. Here's what we tell you in the quick view and also in the summaries of the rest of the chapter:

- **Symbolic Name** of the variable in the form BASE.offset_name. Limited space sometimes compels us to list the name on two lines:

  BASE.
  offset_name

- **O** is the numerical offset named by offset_name.
- **L** is the length of the variable's value in datawords, starting at BASE+0.
- **Access** is the ATU that can receive an MP message containing this CMV and whether the message specifies values to be written in ATU memory (R/W) or merely requests the return of the CMV's dataword as it exists in the ATU (R-only). The table uses NE for near end and FE for far end.
- **Description** is a brief statement of the purpose of the CMV.

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Table 1.CMV Quick View

Symbolic Name	O	L	Access	Description
ADPT.downstream	0	1	ATU-C R/W	Provides DS Rate-adaptive Configuration information. Default: 0x33FF0001
ADPT.downstream	0	1	ATU-R R-only	Contains no information.
ADPT.upstream	1	1	ATU-C R/W ATU-R R-only	The ATU-C provides US rate-adaptive configuration information. The ATU-R contains no information.
ADPT.ds_config	4	1	ATU-C only R/W	New interface- Provides DS Rate-adaptive configuration information (Rate, Margins) Default: 0x63FF0001
ADPT.ds_latency	5	1	ATU-C only R/W	New interface- Provides DS Rate-adaptive configuration information (latency) Default: 0x00407F7F
ADPT.us_config	6	1	ATU-C only R/W	New interface-Provides US Rate-adaptive configuration information. (Rate, Margins) Default: 0x63FF0001
ADPT.us_latency	7	1	ATU-C only R/W	New interface-Provides US Rate-adaptive configuration information. (latency) Default: 0x00407F7F
CNTL.control	0	1	ATU-C R/W	Controls ATU-C state, type of link configuration. (ADPT 4:7 now used see ADPT summary P. 6-14)
CNTL.control	0	1	ATU-R R/W	Controls ATU-R state.
CODE.downstream	0	1	ATU-C R-only ATU-R R-only	Returns DS codeword size and number of FEC checkbytes.

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Table 1.CMV Quick View

Symbolic Name	O	L	Access	Description
CODE.upstream	1	1	ATU-C R-only ATU-R R-only	Returns US codeword size and number of FEC checkbytes.
DIAG.control	0	1	NE ATU-C R/W NE ATU-R R/W	Controls collection and reporting of diagnostic information.
DIAG.flags	1	1	NE ATU-C, NE ATU-R, FE ATU-C, R-only	Returns status of the defect and failure detection flags.
DIAG.flags_latched	2	1	NE ATU-C, NE ATU-R, FE ATU-C R-only	Returns status of latched defect and failure detection flags.
DIAG.rx_intl_hec_cell_count	3	1	NE ATU-C, NE ATU-R, R-only	Returns number of NE HEC-I anomalies in the INTL path.
DIAG.rx_fast_hec_cell_count	4	1	NE ATU-C, NE ATU-R, R-only	Returns number of NE HEC-F anomalies in the fast path.
DIAG.rx_intl_total_cell_count	5	1	ATU-C R-only ATU-R R-only	Keeps count of the total number of cells received in the INTL path. This includes user, idle, unassigned, and cells with bad HEC's.
DIAG.rx_fast_total_cell_count	6	1	ATU-C R-only ATU-R R-only	Keeps count of the total number of cells received in the FAST path. This includes user, idle, unassigned, and cells with bad HEC's.
DIAG.rx_intl_user_cell_count	7	1	NE ATU-C, NE ATU-R, R-only	Returns number of data cells in the Interleave Path delivered at the V-C (ATU-C) or T-R (ATU-R) interface.
DIAG.rx_fast_user_cell_count	8	1	NE ATU-C, NE ATU-R, R-only	Returns number of data cells in the Fast Path delivered at the V-C (ATU-C) or T-R (ATU-R) interface.

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Symbolic Name	O	L	Access	Description
DIAG.flags_1	9	1	ATU-C R-only ATU-R R-only	Returns instantaneous flags for LCD defects.
DIAG.flags_latched_1	10	1	ATU-C R-only ATU-R R-only	Returns latched flags for LCD defects.
DIAG.rx_intl_idle_cell_count	11*	1	NE ATU-C R-only NE ATU-R R-only	Rx intl path idle cell count
DIAG.rx_fast_idle_cell_count	12*	1	NE ATU-C R-only NE ATU-R R-only	Tx Fast path idle cell count
DIAG.rx_intl_unassigned _count	13*	1	NE ATU-C R-only NE ATU-R R-only	Rx intl path unassigned count
DIAG.rx_fast_unassigned _ count	14*	1	NE ATU-C R-only NE ATU-R R-only	Rx fast path unassigned count
DIAG.rx_intl_fifo_overflow	15*	1	NE ATU-C R-only NE ATU-R R-only	Rx intl path overflow count
DIAG.rx_fast_fifo_overflow	16*	1	NE ATU-C R-only NE ATU-R R-only	Rx Fast path overflow
DIAG.(Reserved)[]	17-21	5		
DIAG. near_end_Total_ES_Count	22	1	NE ATU-C, NE ATU-R, R-only	Returns NE errored seconds during the last datapath transfer.

***Anaconda/Diamondback/Eagle Specific CMV**

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Symbolic Name	O	L	Access	Description
DIAG. near_end_Current_Attenuation	23	1	NE ATU-C, NE ATU-R, R-only	Returns NE last measured attenuation.
DIAG. near_end_Previous_Attenuation	24	1	NE ATU-C, NE ATU-R, R-only	Returns NE attenuation measured for 10-sec. period previous to that of current attenuation.
DIAG. near_end_Current_SNR_Margin	25	1	NE ATU-C, NE ATU-R, R-only	Returns the NE last measured SNR margin.
DIAG. near_end_Previous_SNR_Margin	26	1	NE ATU-C, NE ATU-R, R-only	Returns the NE SNR margin measured for 10-sec. period previous to that of current SNR margin.
DIAG.half_db_step_near_end_ current_snr_margin	27	1	NE ATU-C R-only NE ATU-R R-only	
DIAG.half_db_step_near_end_ prvious_snr _margin	28	1	NE ATU-C R-only NE ATU-R R-only	
DIAG.half_db_step_far_end_ previous_snr_margin	29	1	FE ATU-C R-only FE ATU-R R-only	
DIAG.half_db_step_far_end_ previous_snr_margin	30	1	FE ATU-C R-only FE ATU-R R-only	
DIAG.(Reserved)[]	31	1		

***Anaconda/Diamondback/Eagle Specific CMV**

Table 1.CMV Quick View

Symbolic Name	O	L	Access	Description
DIAG.near_end_fcrc_uncorrected _blocks	32	1	NE ATU-C R-only NE ATU-R R-only	Number of NE Received blocks containing uncorrected errors in the Fast path since the beginning of the link
DIAG.near_end_icrc_uncorrected _blocks	33	1	NE ATU-C R-only NE ATU-R R-only	Number of NE Received blocks containing uncorrected errors in the Intl path since the beginning of the link.
DIAG.near_end_good_blocks	34	1	NE ATU-C R-only NE ATU-R R-only	Number of NE Received good blocks since the beginning of the link.
DIAG.tx_intl_total_cell_count	35*	1	ATU-C ATU-R	Returns the number of data cells in the interleave path transmitted to the V-C (ATU-C) or RT (ATU-R) interface
DIAG.tx_fast_total_cell_count	36*	1	ATU-C ATU-R	Returns the number of data cells in the fast path transmitted to the V-C (ATU-C) or RT (ATU-R) interface
DIAG.tx_intl_idle_cell_count	37	1	NE ATU-C R-only NE ATU-R R-only	Tx intl lantency path Idle cell count*
DIAG..tx_fast_idle_cell_count	38	1	NE ATU-C R-only NE ATU-R R-only	Tx fast path Idle cell count*
DIAG..tx_intl_short_cell_count	39*	1	ATU-C ATU-R	Returns the number of short cells transmitted in the inleave path
DIAG..tx_fast_short_cell_count	40*	1	ATU-C ATU-R	Returns the number of short cells transmitted in the fast path
DIAG.regular_bitswap_msg_count	41	1	ATU-C R-only ATU-R R-only	Returns the count of regular bitswap messages received.
DIAG.extented_bitswap_msg _ count	42	1	ATU-C R-only ATU-R R-only	Returns the count of extended bitswap messages received.

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Symbolic Name	O	L	Access	Description
DIAG.utc_msg_count	43	1	ATU-C R-only ATU-R R-only	Returns the count of bitswap UTC messages received.
DIAG.ds_bitswap_count	44	1	ATU-C R-only ATU-R R-only	Returns the count of downstream bitswaps performed.
DIAG.us_bitswap_count	45	1	ATU-C R-only ATU-R R-only	Returns the count of upstream bitswaps performed.
DIAG. far_end_Total_ES_Count	46	1	FE ATU-C R-only	Returns the FE errored seconds during the last datapath transfer.
DIAG. far_end_Current_Attenuation	47	1	FE ATU-C R-only	Returns the FE last measured attenuation.
DIAG. far_end_Previous_Attenuation	48	1	FE ATU-C R-only	Returns FE attenuation measured for 10-sec. period previous to the one of the current attenuation.
DIAG. far_end_Current_SNR_Margin	49	1	FE ATU-C R-only	Returns the FE last measured SNR margin.
DIAG. far_end_Previous_SNR_Margin	50	1	FE ATU-C R-only	Returns FE SNR margin measured for 10-sec. period previous to one of current SNR margin.
DIAG.near_end_Rcvd_Blocks	51	1	NE ATU-C, NE ATU-R R-only	Returns total number of NE received blocks since start of link.
DIAG. near_end_Xmitted_Blocks	52	1	NE ATU-C, NE ATU-R R-only	Returns total number of NE transmitted blocks since start of link.
DIAG. near_end_Corrected_Blocks	53	1	NE ATU-C, NE ATU-R R-only	Returns number of NE received blocks with corrected errors since start of link.
DIAG. near_end_Uncorr_Blocks	54	1	NE ATU-C, NE ATU-R R-only	Returns number of NE received blocks with uncorrectable errors since start of link.
DIAG.far_end_Rcvd_Blocks	55	1	ATU-C R-only	Returns total number of FE received blocks since start of link.
DIAG. far_end_Xmitted_Blocks	56	1	ATU-C R-only	Returns total number of FE transmitted block since start of link.

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Symbolic Name	O	L	Access	Description
DIAG. far_end_Corrected_Blocks	57	1	ATU-C R-only	Returns number of FE received blocks with corrected errors since start of link.
DIAG.far_end_Uncorr_Blocks	58	1	ATU-C R-only	Returns number of FE received blocks with uncorrectable errors since start of link.
DIAG.tx_intl_long_cell_count	59*	1	ATU-C ATU-R	Returns the number of long cells transmitted in the intl path
DIAG.tx_fast_long_cell_count	60*	1	ATU-C ATU-R	Returns the number of long cells transmitted in the fast path
DOPT.mux_option	0	1	ATU-C R/W	Specifies Interleave or Fast Path.
DOPT.simplex_bytes	1	1	ATU-C R/W	Specifies full-rate DS data rates.
DOPT.duplex_bytes	2	1	ATU-C R/W	Specifies downstream data rates in duplex path (LS) for 4 options.
DOPT.fast_check_bytes	3	1	ATU-C R/W	Specifies number of fast-path check-bytes.
DOPT.intl_check_bytes	4	1	ATU-C R/W	Specifies number of interleave-path checkbytes.
DOPT.intl_depth	5	1	ATU-C R/W	Specifies interleave depth.
DOPT. symbols_per_codeword	6	1	ATU-C R/W	Specifies symbols/codeword.
DOPT.required_margin	7	1	ATU-C R/W	Specifies required SNR margin.
FLAG.mask	0	1	ATU-C, ATU-R R/W	Sets events on which an ATU will trigger a Flag Signal.
INFO.RT_serial_number[]	0-7	8	ATU-C R-only ATU-R R/W	Reads ATU-R Serial Number.
INFO.RT_vendor_ID	8	1	ATU-C R-only ATU-R R/W	Reads ATU-R modem Vendor ID.
INFO.RT_version_number	9	1	ATU-R R-only	Reads ATU-R Version Number.
INFO.RT_fw_version	10	1	ATU-R R-only ATU-C R-only (if G.hs is used)	Reads ATU-R firmware version.

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Symbolic Name	O	L	Access	Description
INFO.CO_fw_version	11	1	ATU-C R-only ATU-R R-only (if G.hs is used)	Reads ATU-C firmware version.
INFO.candidate_number	12	1	ATU-C, ATU-R R-only	Reads candidate number of modem's firmware version.
INFO.ANSI_rt_ver	13	1	ATU-C R-only ATU-R R-only	Contains the ANSI Vendor ID of the ATU-R. The ID is exchanged during link initiation.
INFO.ANSI_co_ver	14	1	ATU-C R-only ATU-R R-only	Contains the ANSI Vendor ID of the ATU-C. The ID is exchanged during link initiation.
INFO.Chips_ver	15	1	ATU-C R-only ATU-R R-only	Returns the Version Number of 6438/6449 and flash/SRAM
INFO.itu_rt_ver INFO.itu_rt_ver	17 18	2	ATU-C R-only ATU-R R-only	ITU Vendor ID (8bytes) of ATU-R
INFO.itu_co_ver INFO.itu_co_ver	19 20	2	ATU-C R-only ATU-R R-only	ITU Vendor ID (8bytes) of ATU-C
INFO.itu_rt_eoc_ver INFO.itu_rt_eoc_ver	21 22	2	ATU-C R-only ATU-R R/W	ITU Vendor ID to be exchanged over EOC for G.hs links
INTL.downstream	0	1	ATU-C, ATU-R R-only	Reads current DS interleave depth.
INTL.upstream	1	1	ATU-C, ATU-R R-only	Reads current US interleave depth.
MASK.downstream[]	0-7	8	ATU-C R/W	Enables or disables a specified set of tones in the DS datapath.
MASK.upstream	8	1	ATU-C R/W ATU-R R/W	Enables or disables a specified set of tones in the US datapath.
MASK.	9	1	ATU-C R/W ATU-R R/W	Enables or disables a specified set of tones in the US datapath.
OPTN.options	0	1	ATU-C, ATU-R R/W	Discovers if optional features are on modem, used or specifies use.
OPTN.bitswap	1	1	ATU-C, ATU-R R/W	Configurations for the bitswap feature.
OPTN.utopia	2	1	ATU-C, ATU-R R/W	Configures ATM/UTOPIA.

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Symbolic Name	O	L	Access	Description
OPTN.fdq	3	1	ATU-C R/W ATU-R R/W	Enables or disables FDQ.
OPTN.adsl_standard	4	1	ATU-R R/W	User-programmed register to select ADSL standard options for ATU-R.
OPTN.cpr_01	5	1	ATU-C R/W ATU-R R/W	User-programmed register used for CPR software work-arounds and miscellaneous information.
OPTN.930	6	1	ATU-C R/W ATU-R R/W	Selects “Normal” or “Standby” mode
OPTN.atm_fifo	7*	1	ATU-C R/W ATU-R R/W	Configures the FIFO’s of the AD6438. (Bits 15:0 are reserved for Anaconda/Diamondback applications)
OPTN.(Reserved)	8-12	5		
OPTN.lpbk_config	13*	1	ATU-C ATU-R	Set up general Loopback features such as ATM addresses, Utopia level, Tx mode, ADSL and ATM scrambling
OPTN.lpbk_rate	14*	1	ATU-C ATU-R	Set up Fast and intl latency path rates in Loopback mode
OPTN.atm_fifo_new	15*	1	ATU-C ATU-R	This sets up the Tx and Rx FIFO sizes in each latency path
PFCL.status	0	1	ATU-C, ATU-R R-only	Returns the Tx and Rx training profiles currently in use, and the number of fast retrains executed so far.
PFCL.control	1	1	ATU-C, ATU-R R/W	Sets fast retrain margin to be used during profile selection.
PFRX.profilenum[]	0-7	8	ATU-C, ATU-R R-only	Returns information about Rx profile 0-7.
PFTX.profilenum[]	0-7	8	ATU-C, ATU-R R-only	Returns information about Tx profile 0-7.
PSDM.config	0	1	ATU-C R/W ATU-R R/W	Restricts ATU output power to a new maximum PSD.

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Symbolic Name	O	L	Access	Description
PSDM.actual	1	1	ATU-C, ATU-R R-only	Reads the current PSD.
RATE.actual	0	1	ATU-C, ATU-R R-only	Returns the current US and DS data rates in bytes per symbol.
RATE.maximum	1	1	ATU-C, ATU-R R-only	Returns the maximum possible data rates.
RXDA.(reserved)	0	1		
RXDA.data[]	1-2	2	ATU-C, ATU-R R-only	Receives message over EOC from a TXDA.data.
RXDA.(reserved)[]	3-9	8		
RXDA.clear_EOC	10	1	ATU-C R-only ATU-R R-only	Receives a message transmitted over the EOC from a TXDA.data.
RXDA.mailbox	11	1	ATU-C R/W, ATU-R R/W	Notifies the recipient ME that a message is in RXDA.data and RXDA.clear_EOC
STAT.status	0	1	NE ATU-C R-only NE ATU-R R-only	Requests ATU status dataword.
STAT. initialization_failure_codes	1	1	ATU-C, ATU-R R-only	Requests initialization failure code.
STAT.930	3	1	ATU-C R-only	0=ModemisinNormalmode (Refer to Bit 4 of OPTN.930) 1=ModemisinStandbymode (Refer to Bit 4 of OPTN.930)
STAT.lpbk_rate	4*	1	ATU-C ATU-R	This reflects the actual fast and intl latency path rates in the UTOPIA loopback mode. The firmware will override invalid user settings in OPTN.lpbk_rate with valid defaults
STAT.atm_fifo	5*	1	ATU-C ATU-R	This reflects the actual Tx and Rx FIFO sizes in each latency path. The firmware will override invalid user settings in OPTN.atm_fifo with valid defaults

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Symbolic Name	O	L	Access	Description
TEST.control	0	1	ATU-C, ATU-R R/W	Starts or stops power on one bin or on all bins.
TEST.receive_power[]	1-31	31	ATU-C R-only	Returns measured power on one of 30 US and 1 DS bin.
TEST.receive_power[]	32-255	224	ATU-R R-only	Returns measured power on one of 224 DS bins.
TONE.upstream[]	0-30	31	ATU-C R-only	Returns tone characteristics on one of 31 US bins.
Reserved[]	31-62	32		
TONE.downstream[]	63-287	225	ATU-R R-only	Returns tone characteristics on one of 225 DS bins.
TXDA.(reserved)	0	1		
TXDA.data[]	1-2	2	ATU-C, ATU-R R/W	Transmits a message over the EOC to an RXDA.data.
TXDA.(reserved)[]	3-9	7		
TXDA.clear_EOC	10	1	ATU-C R/W ATU-R R/W	Receives a message transmitted over the EOC from a TXDA.data.
TXDA.mailbox	11	1	ATU-C, ATU-R R/W	Notifies the sender ME that a message is not in TXDA.data and RXDA.clear_EOC.
UOPT.mux_option	0	1	ATU-C R/W	Specifies Interleave or Fast Path.
UOPT.simplex_bytes	1	1	Reserved.	
UOPT.duplex_bytes	2	1	ATU-C R/W	US data rates, 4 options.
UOPT.fast_check_bytes	3	1	ATU-C R/W	Number of fast-path checkbytes, 4 options.
UOPT.intl_check_bytes	4	1	ATU-C R/W	Number of interleave-path checkbytes, 4 options.

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Symbolic Name	O	L	Access	Description
UOPT.intl_depth	5	1	ATU-C R/W	Interleave depth, 4 options.
UOPT. symbols_per_codeword	6	1	ATU-C R/W	Symbols/codeword, 4 options.
UOPT.required_margin	7	1	ATU-C R/W	Required SNR margin.

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Anaconda/Diamondback/Eagle Specific CMV Quick Locator

CMV Name	Offset	Page
DIAG.rx_intl_idle_cell_count	11	67
DIAG.rx_fast_idle_cell_count	12	68
DIAG.rx_intl_unassigned_cell_count	13	69
DIAG.rx_fast_unassigned_cell_count	14	70
DIAG.rx_intl_fifo_overflow	15	71
DIAG.rx_fast_fifo_overflow	16	72
DIAG.tx_intl_total_cell_count	35	76
DIAG.tx_fast_total_cell_count	36	77
DIAG.tx_intl_idle_cell_count	37	78
DIAG.tx_fast_idle_cell_count	38	79
DIAG.tx_intl_short_cell_count	39	80
DIAG.tx_fast_short_cell_count	40	81
DIAG.tx_intl_long_cell_count	59	82
DIAG.tx_fast_long_cell_count	60	83
OPTN.lpbk_config	13	137
OPTN.lpbk_rate	14	139
OPTN.atm_fifo	15	140
STAT.lpbk_rate	4	185
STAT.atm_fifo	5	186

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Anaconda/Diamondback/Eagle CMV Overview

Summary

The following CMVs (Configuration Management Variables) utilize additional functional capabilities that were not previously available.

New Tx UTOPIA DIAG (diagnostic) CMVs

DIAG.tx_intl_total_cell_count (offset 35)

DIAG.tx_fast_total_cell_count (offset 36)

DIAG.tx_intl_idle_cell_count (offset 37)

DIAG.tx_fast_idle_cell_count (offset 38)

DIAG.tx_intl_short_cell_count (offset 39)

DIAG.tx_fast_short_cell_count (offset 40)

DIAG.tx_intl_long_cell_count (offset 59)

DIAG.tx_fast_long_cell_count (offset 60)

Definitions:

Short Cells

A short-cell error occurs when the 'Tx SOC' UTOPIA control line (an input) is re-asserted before the full 53 bytes on an ATM cell have been transmitted.

Long Cells

A long-cell error occurs when the 'TxENB' UTOPIA control line (an input) remains asserted after the full 53 bytes of an ATM cell have been transferred and the 'TxSOC' UTOPIA control line (an input) is not re-asserted on the following byte.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Discarded Tx Cells

When data is said to be discarded on the Tx UTOPIA interface, it means that the data does not remain in the associated Tx FIFO long enough to make it out onto the ADSL line. It is overwritten by subsequent incoming Tx ATM cell data as it becomes available on the Tx UTOPIA interface.

New Rx UTOPIA DIAG (diagnostic) CMVs

There are 6 DIAG.Rx offsets that remain unaltered for Anaconda, Diamondback, and Eagle. The names have changed slightly to make them more descriptive. These CMVs will be descriptive. These CMVs will be described in further detail later in this section. They are:

DIAG.rx_intl_hec_cell_count (offset 3)

DIAG.rx_fast_hec_cell_count (offset 4)

DIAG.rx_intl_total_cell_count (offset 5)

DIAG.rx_fast_total_cell_count (offset 6)

DIAG.rx_intl_user_cell_count (offset 7)

DIAG.rx_fast_user_cell_count (offset 8)

For the previous 918 and 930 chipsets, DIAG offsets 11 through 20 were reserved. The combination of Rx UTOPIA cell counts available here provided improved user visibility into the types of cell-level errors being experienced in the physical layer.

The New Rx UTOPIA DIAG CMVs are as follow:

DIAG.rx_intl_idle_cell_count (offset 11)

DIAG.rx_fast_idle_cell_count (offset 12)

DIAG.rx_intl_unassigned_cell_count (offset 13)

DIAG.rx_fast_unassigned_cell_count (offset 14)

DIAG.rx_intl_fifo_overflow (offset 15)

DIAG.rx_fast_fifo_overflow (offset 16)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Associated CMVs: OPTN.atm_fifo_new

In Anaconda and Eagle based modem systems, the receiver always discards the following types of cells.

a. Idle cells

b. Cells that cause the Rx FIFO to overflow

Separate counters for these cell types are available in the Rx UTOPIA DIAG. CMVs.

The receiver can also be configured to discard or not to discard the following types of cells:

c. Cells with invalid HECs

d. Cells received while in the ATM pre-sync state

e. Unassigned cells

Separate counters are available for cells with invalid HECs and Unassigned cells. Whether or not these cell types are discarded, these counters always increment when the associated cell types are detected. If they are configured not to be discarded, the associated counts are included in the Rx user cell count as well.

Definitions:

Discarded Rx Cells

When data is said to be discarded on the Rx UTOPIA interface, it means that the data does not remain in the associated Rx FIFO long enough to make it out onto the RX UTOPIA interface. It is over written by subsequent incoming Rx ATM cell data as it becomes available over the ADSL link.

Unassigned Cells

Unassigned cells have a similar functionality for an ATM layer device as the Idle cells have for the TC sub-layer of a PHY device. They are used for cell rate decoupling in the ATM layer. The transmission of Unassigned cells from an ATM layer device requires no particular settings or actions from the TC sub-layer device (DTIR).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

New Tx/Rx UTOPIA 'OPTN' CMVs

All three of these CMVs can be used to configure UTOPIA loopback prior to entering the UTOPIA loopback mode. The OPTN.atm_fifo_new (offset 15) CMV should also be used in regular end-to-end link operations to configure the Tx and Rx fifos for the intl and fast ADSL latency paths. This CMV (OPTN.atm_fifo_new (offset 15) replaces OPTN.atm_fifo (offset 7) bits 15:0 which were used on previous 918 and 930 based products for the same purpose. OPTN.atm_fifo (offset 7) bits 15:0 are now unused.
The new CMVs are:

OPTN.lpbk_config (offset 13) (Refer to application note ANCMV-05)

OPTN.1pbk_rate (offset 14) (Refer to application note ANCMV-05)

OPTN.atm_fifo_new (offset 15)

Note: OPTN.lpbk_config (offset 13) and OPTN.1pbk_rate (offset 14) are intended to be used in conjunction with the STAT.lpbk_rate (offset 4) and STAT.lpbk_rate (offset 5) CMVs. Refer to application note ANCMV-05 in this manual for further details.

New Tx/Rx UTOPIA 'STAT' CMVs

The user is able to configure the ATM Tx/Rx fifos (regular link and loopback) and select the payload levels on the intl and fast ADSL latency paths (loopback only) using OPTN.atm_fifo_new (offset 15) and OPTN.lblk_rate (offset 14) respectively. If the user configures invalid settings in these CMVs, the firmware will override them with sensible defaults. The STAT.atm_fifo (offset 5) CMVs and STAT.lpbk_rate (offset 4) CMV indicates the actual settings applied, regardless of whether they represent the original user settings or overridden defaults.
The new STAT CMVs are:

STAT.lpbk_rate (offset 4) (Refer to application note ANCMV-05)

STAT.atm_fifo (offset 5) (Refer to application note ANCMV-05)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

ADPT (Rate Adapted)

Summary

Name	O	L	Access	Description
ADPT.downstream	0	1	ATU-C only R/W	Provides DS Rate-adaptive configuration information. Default: 0x33FF0001
ADPT.upstream	1	1	ATU-C only R/W	Provides US Rate-adaptive configuration information. Default: 0x60FF0001
ADPT.ds_config	4	1	ATU-C only R/W	New interface- Provides DS Rate-adaptive configuration information (Rate, Margins) Default: 0x63FF0001
ADPT.ds_latency	5	1	ATU-C only R/W	New interface- Provides DS Rate-adaptive configuration information (latency) Default: 0x00407F7F
ADPT.us_config	6	1	ATU-C only R/W	New interface-Provides US Rate-adaptive configuration information. (Rate, Margins) Default: 0x63FF0001
ADPT.us_latency	7	1	ATU-C only R/W	New interface-Provides US Rate-adaptive configuration information. (latency) Default: 0x00407F7F

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 2 ATU-C ADPT.downstream (ADPT offset 0)

Bits	Name	Description
8:0	Min DS Data Rate	The minimum number of DS data bytes per ADSL frame (symbol). Zero is not allowed. Default: 0x1
15:9	Interleave Depth	The interleave depth in bytes. If you are specifying Fast Path, this value does not get used. Default: 0x0
24:16	Max DS Data Rate	The maximum number of DS data bytes per ADSL frame. Default: 0x1FF
25	Coding	0 — No coding. 1 — Use coding. (Default)
26	Path Type	0 — Use Interleave Path DS. (Default) 1 — Use Fast Path DS.
31:28	SNR Margin	The DS margin requirement in dB. • The range is 0 through 15 dB in 1 dB steps. This will not include any gain from the coding.

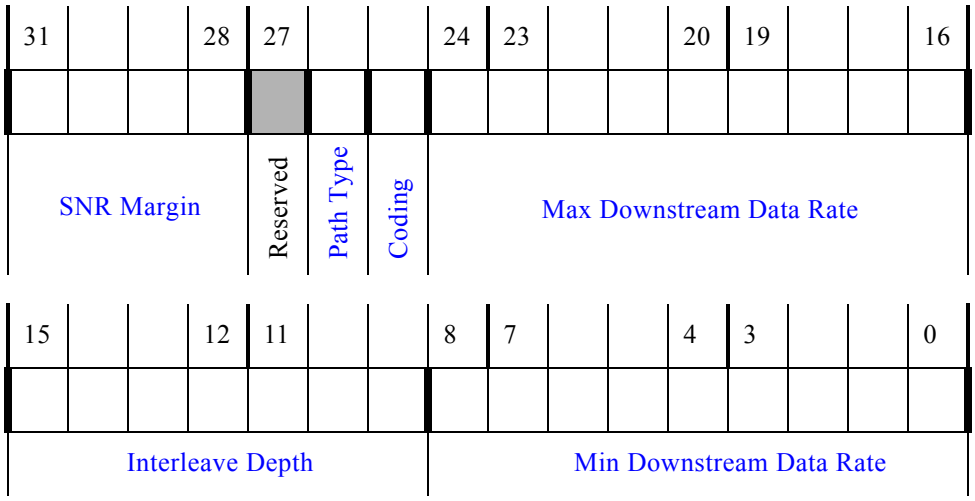

Figure 1. ATU-C ADPT.downstream (ADPT offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 3 ATU-C ADPT.upstream (ADPT offset 1)

Bits	Name	Description
8:0	Min US Data Rate	The minimum number of US data bytes per ADSL frame. Default: 0x1
15:9	Interleave Depth	The interleave depth in bytes. If you are specifying Fast Path, this value does not get used. Default: 0x0
24:16	Max US Data Rate	The maximum number of US data bytes per ADSL frame. Default: 0x1FF
25	Coding	0 — No coding. 1 — Use coding. (Default)
26	Path Type	0 — Use Interleave Path US. (Default) 1 — Use Fast Path DS.
31:28	SNR Margin	The US margin requirement in dB. • The range is 0 through 15 dB in 1 dB steps. This will not include any gain from the coding.

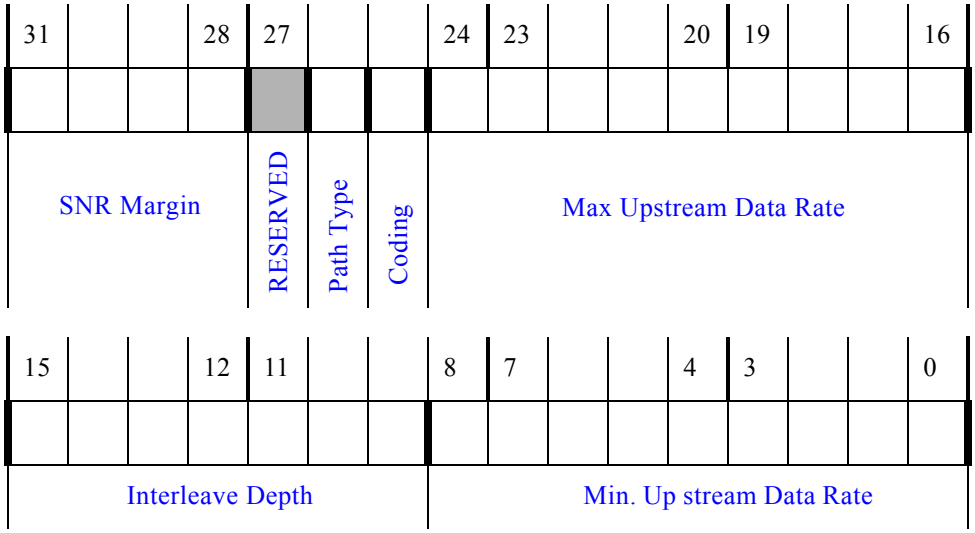

Figure 2. ATU-C ADPT.upstream (ADPT offset 1)

Table 4 ATU-C ADPT.ds_config (ADPT offset 4)

Bits	Name	Description
8:0	Min DS Data rate	The minimum number of DS data bytes per ADSL frame. Default: 0x1
15:9	RESERVED	Default: 0x0
24:16	Max DS Data rate	The maximum number of DS data bytes per ADSL frame. Default: 0x1FF
25	DS coding	0- No coding 1- Use coding (Default)
26	Path Type	0 - Use Interleave Path DS (Default) 1 - Use Fast Path DS
27	RESERVED	Default: 0x0
31:28	DS Margin	DS Margin requested. This will include any gain from coding. Default: 0x6

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Figure 3. ATU-C ADPT.ds_config (ADPT offset 4)

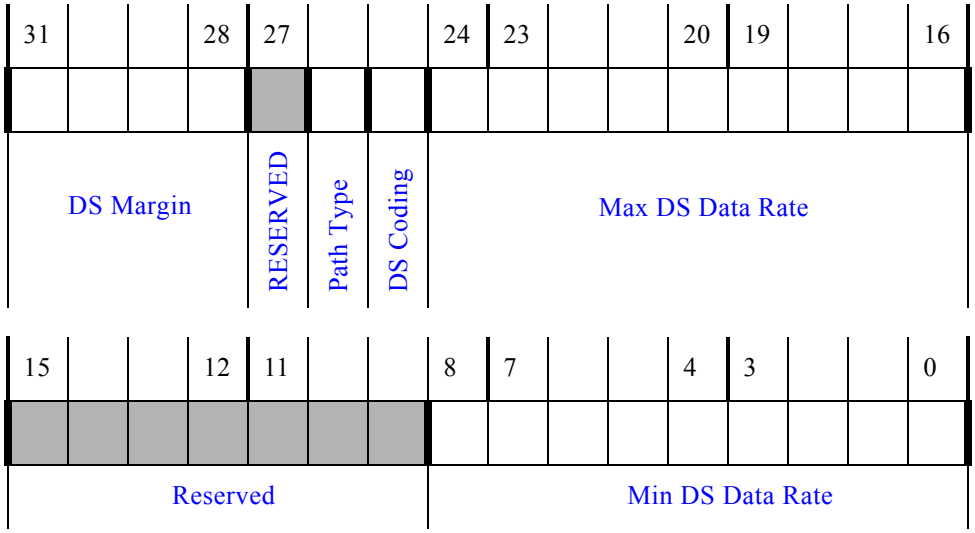

Table 5 ATU-C ADPT.ds_latency (ADPT offset 5)

Bits	Name	Description
6:0	Maximum DS latency	The maximum DS latency measured in ADSL frames (0.25ms). Default: 0x7F
7	RESERVED	Default: 0x0
14:8	Maximum DS symbols per codeword (Smax)	Maximum requested DS symbols per codeword (Smax). Default: 0x7F
15	RESERVED	Default: 0x0
22:16	Maximum DS interleave depth (Dmax)	Maximum DS interleave depth (Dmax). Default: 0x40
30:23	RESERVED	Default: 0x0
31	ENABLE NEW ADPT CMVS	Set this bit to 1 to enable the use of the New Interface (ADPT 4-7), for US and DS. Set this bit to 0 to enable the use of the Old Interface (ADPTs 0-1), for US and DS. Default: 0x0

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Figure 4. ATU-C ADPT.ds_latency (ADPT offset 5)

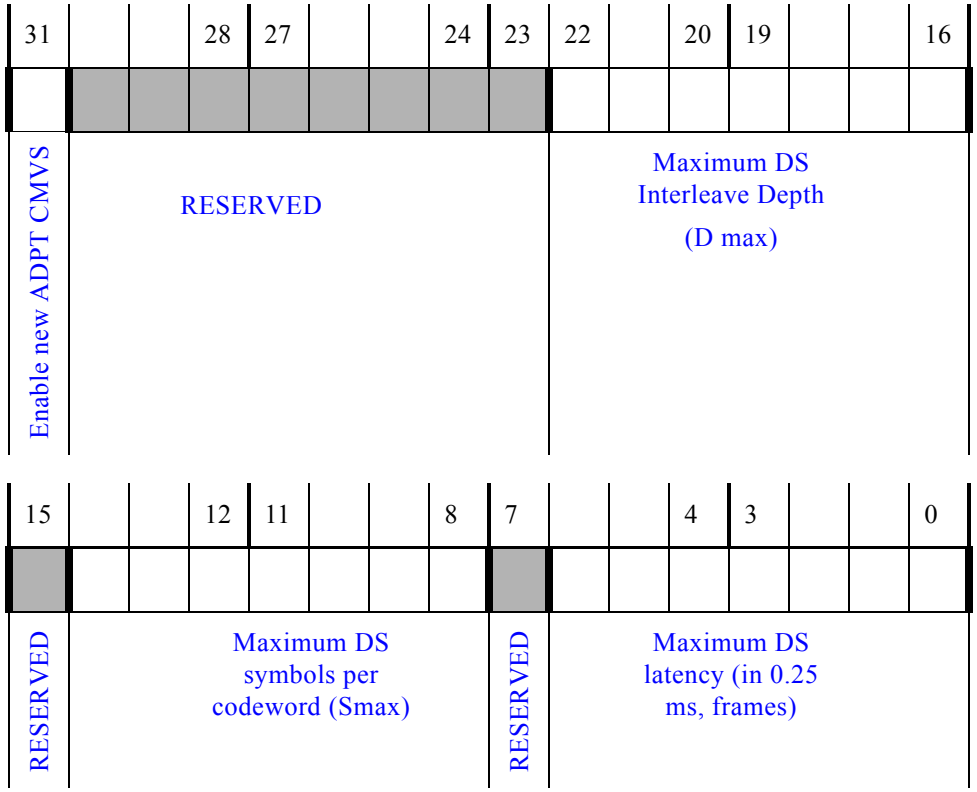

Table 6 ATU-C ADPT.us_config (ADPT offset 6)

Bits	Name	Description
8:0	Min US Data Rate	The minimum number of US data bytes per ADSL frame. Default: 0x1
15:9	RESERVED	Default: 0x0
24:16	Max US Data Rate	The maximum number of US data bytes per ADSL frame. Default: 0x1FF
25	US coding	0 - No Coding 1 - Use Coding (Default)
26	Path Type	0 - Use Interleave path US (Default) 1 - Use Fast path US
27	RESERVED	Default: 0x0
31:28	US Margin	US Margin requested. This will include any gain from coding. Default: 0x6

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

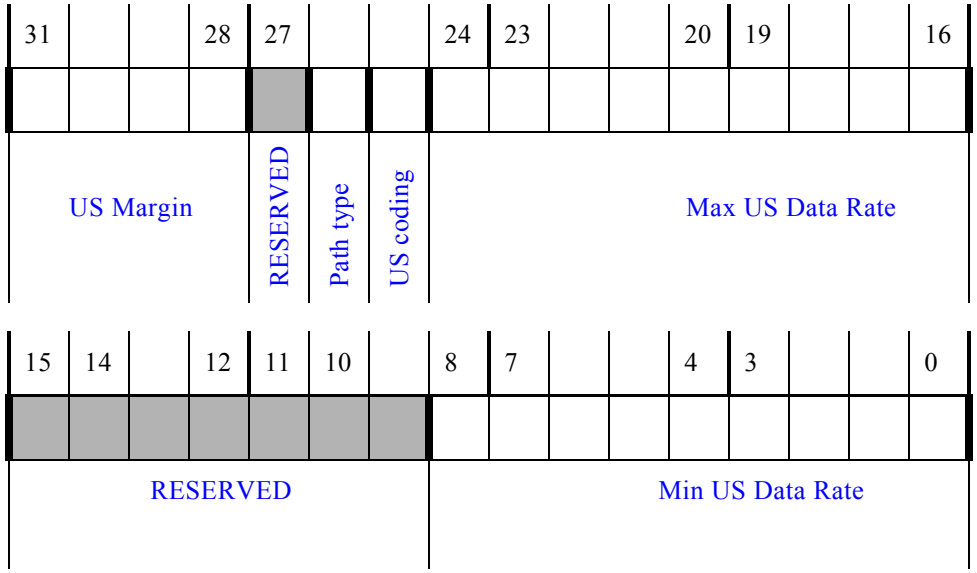

Figure 5. ATU-C ADPT.us_config (ADPT offset 6)

Table 7 ATU-C ADPT.us_latency (ADPT offset 7)

Bits	Name	Description
6:0	Maximum US latency	The Maximum requested US latency measured in ADSL frames (0.25ms). Default: 0x7F
7	RESERVED	Default: 0x0
14:8	Maximum US symbols per codeword (Smax)	The Maximum requested symbols per codeword (Smax). Default: 0x7F
15	RESERVED	Default: 0x0
22:16	Maximum US interleaver depth	TheMaximum requested Interleavedepth(Dmax). Default: 0x40
31:23	RESERVED	Default: 0x0

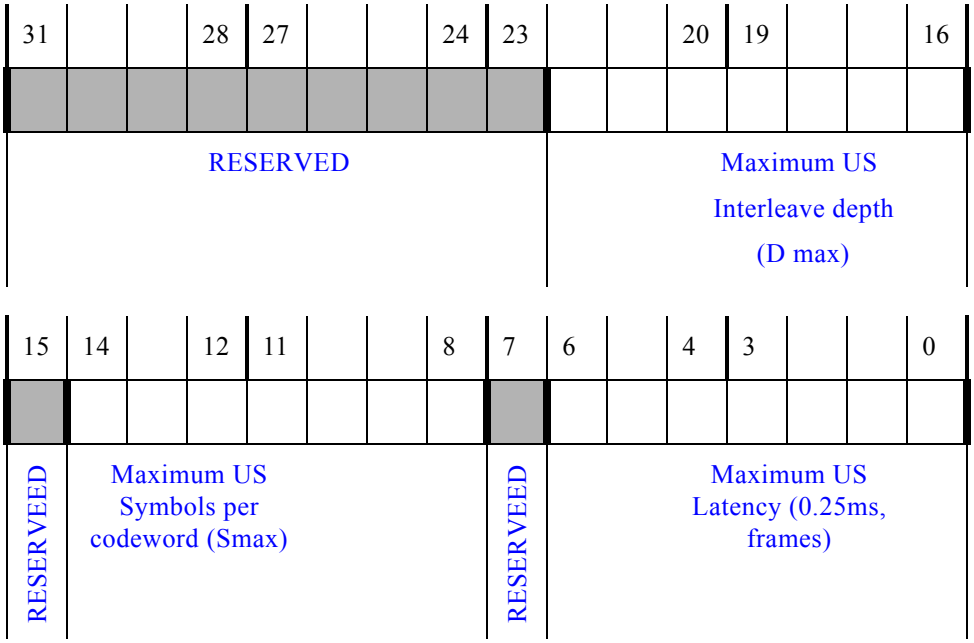

Figure 6. ATU-C ADPT.us _latency (ADPT offset 7)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

If you choose Rate-adaptive configuration, then the ME must use ADPT CMVs to provide configuration information to the ATU-C. These CMVs are only valid at the ATU-C.

Current/Old Interface (available in all versions of code)

If you are using the Old Interface, you must set up ADPT offsets **0** and **1**. The SNR margin should be adjusted for coding gain as discussed in Chapter 4.

New Interface (available in versions 3.1 and later)

If you are using the New Interface, you must set up ADPT offsets 4-7. The code will calculate data rates, coding parameters, and interleave depth in order to achieve the requested margin and latency.

Notes

1. Failure of the ATUs to achieve the minimum data rates will result in an initialization failure and will prevent the ATUs from entering normal operation.
2. If you decide to use Rate-adaptive configuration and the ME does not properly and completely set ADPT field values, the result of the initialization will be undefined.
3. You can convert a data rate from bytes per ADSL frame into bits per second by using:

X bytes per frame * 8 bits per byte * 4000 frames per second = Y bits per seconds

Related CMVs

The results of the negotiation and the established link parameters are available in these CMVs: RATE, CODE, INTL, and STAT.

For Explicit-rate configuration, use DOPT and UOPT.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

CNTL (Control)

Summary

Name	O	L	Access	Description
CNTL.control	0	1	ATU-C R/W	Controls the state of an ATU-C and sets the type of configuration of its links. Default: 0x00000042
			ATU-R R/W	Controls the state of an ATU-R. Default: 0x0

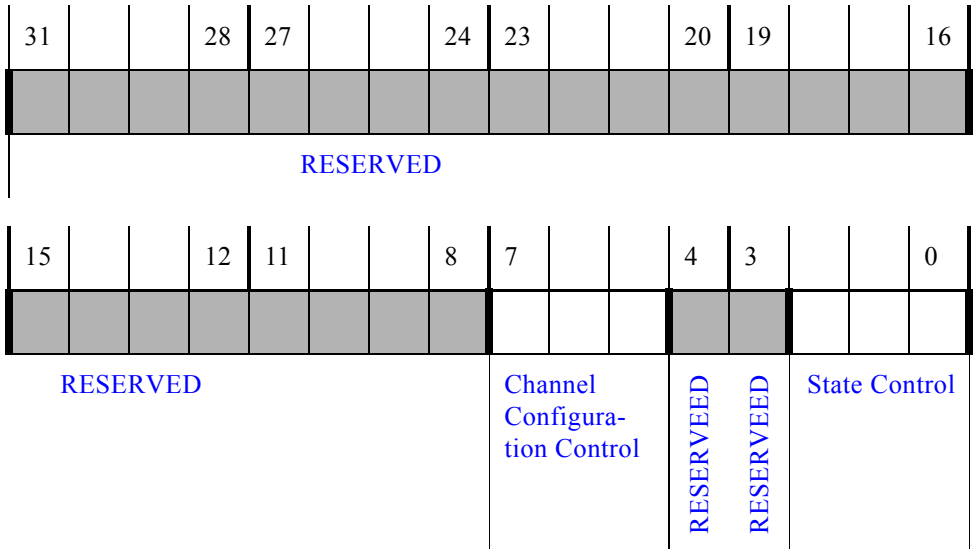

Figure 7. ATU-C CNTL.control (CNTL offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 8 ATU_C CNTL.control (CNTL offset 0)

Bits	Name	Description		
2:0	State Control Field	This field specifies an ATU-C change of state. Default: 0x2		
		Binary	**Hex**	**Description**
		011	0x3	Reserved
		100	0x4	Enter C-TEST-SIGNAL.
		101	0x5	Enter C-TEST-HW. Perform Hardware Register Tests. The ME should wait at least 5 seconds after sending the CNTL before reading the results via STAT.
		110	0x6	Enter C-TEST-LOOPBACK.
		111	0x7	Reserved.
4:3	Reserved	Default 0x0		
7:5	Channel Configu-ration Control Field	This field specifies the type of link configuration Default 0x2		
		Binary	**Hex**	**Description**
		000	0x0	Use Explicit_rate Configuration
		001	0x1	Reserved
		010	0x2	Used Rate_adapted Configuration
7:5	Channel Configu-ration Control Field	This field specifies the type of link configuration Default 0x2		
		Binary	**Hex**	**Description**
		011-111	0x3-0x7	Reserved

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 9 ATU-R CNTL.control (CNTL offset 0)

Bits	Name	Description		
2:0	State Control Field	This field specifies an ATU-R change of state. Default: 0x2		
		Binary	**Hex**	**Description**
		000	0x0	Software reset. Enter R-IDLE (reset), remain there for 1 second, and enter R-ACT-REQ or R-TONES-REQ. See 010.
		001	0x1	Enter and stay in R-IDLE (cmv) until instructed otherwise (only valid within one second of reset).
		010	0x2	Enter R-ACT-REQ or R-TONES-REQ based on configuration.
		011	0x3	Reserved.
		100	0x4	Enter R-TEST-SIGNAL.
		101	0x5	Enter R-TEST-HW. Perform Hardware Register Tests. The ME should wait at least 5 seconds after sending the CNTL before reading the results via STAT.
		110	0x6	Enter R-TEST-LOOPBACK.
2:0	State Control	**Binary** 111	**Hex** 0x7	Place the ATU-R into Lite Mode. It must be an AD20MSP918. Note: Use this field only when the ATU-C is an AD20MSP910 in Lite Mode. Otherwise, OPTN Offset 4 is the proper CMV for initiating a Lite Mode link.
31:3	Reserved	Default 0x0		

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

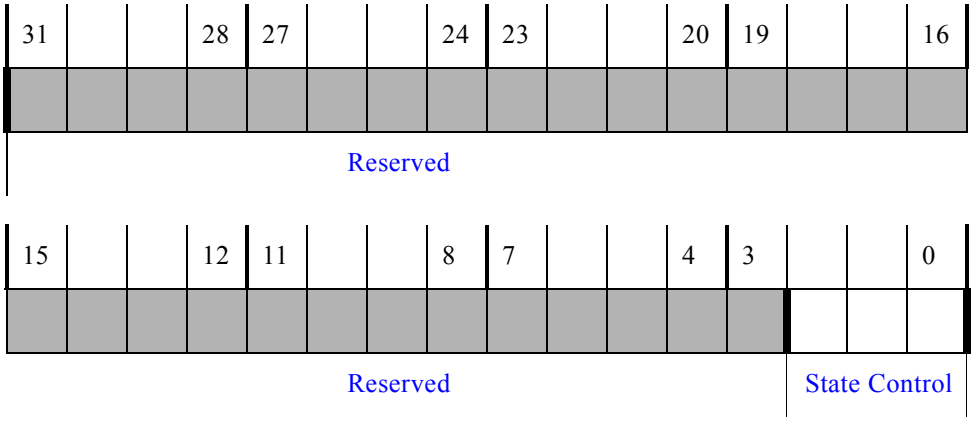

Figure 8. ATU-R CNTL.control (CNTL offset 0)

Usage

An ME uses CNTL to bring about a change of state in a modem. You may find state descriptions and state diagrams in Chapter 2.

An ME changes the state of a modem for two main reasons:

1. Link initialization. Refer to Chapter 4 for these details.
2. Testing. Refer to Chapter 5.

Notes

1. The contents of the State Control Field give the desired state of the ATU. The actual state is available in STAT.status (Offset 0).
2. Transition to IDLE and TEST disables the current data links.

Related CMVs

ADPT

Transmits information for Rate-adaptive configuration, interleaving and coding to an ATU when it is in IDLE.

OPTN

Gives configuration parameters for the TEST-LOOPBACK state.

STAT

Obtains the results of testing when the modem is in IDLE after a test.

TEST

Sets and obtains signal parameters for a modem that is in TEST-SIGNAL state.

UOPT, DOPT

Transmit information for Explicit-rate configuration to an ATU-C when it is in IDLE.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

CODE

Summary

Name	O	L	Access	Description
CODE.downstream	0	1	ATU-C R-only ATU-R R-only	Returns the codeword size and number of FEC checkbytes in use on the ATU's DS link. Default: 0x0
CODE.upstream	1	1	ATU-C R-only ATU-R R-only	Returns the codeword size and number of FEC checkbytes in use on the ATU's US link. Default: 0x0

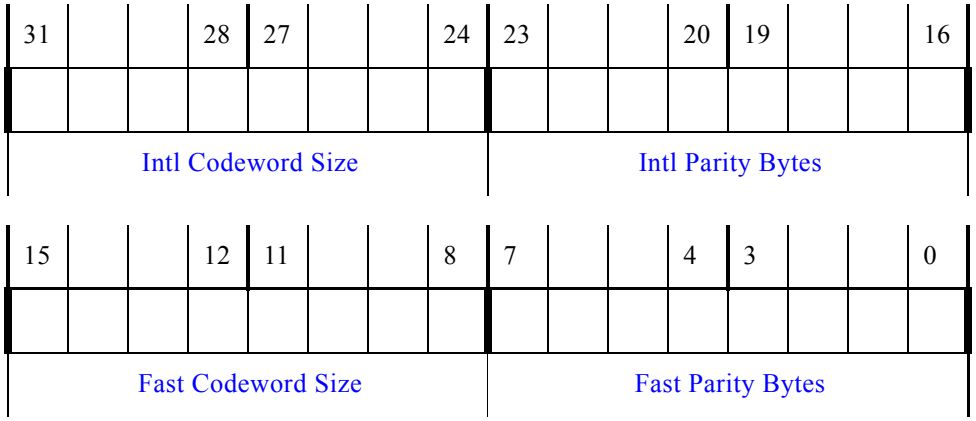

Figure 9. ATU-C/ATU-R CODE.downstream (CODE offset 0) and CODE.upstream (CODE offset 1).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 10 ATU-C / ATU-R CODE.downstream (CODE offset 0) and CODE.upstream (CODE offset 1).

Bits	Field Name	Description
7:0	Fast Parity Bytes	The number of checkbytes currently in use in the Fast path codeword.
15:8	Fast Codeword Size	The number of Fast path bytes per codeword. NOTE: If the link is in Interleave path, then the Fast Codeword Size Field has these values: 1 for Framing Modes 0, 1, 2 0 for Framing Mode 3
23:16	Intl Parity Bytes	The number of checkbytes currently in use in the Interleave-path codeword.
31:24	Intl Codeword Size	The number of Interleave path bytes per codeword. NOTE: If the link is in Fast path, then the Intl Codeword Size Field has these values: 1 for Framing Modes 0, 1, 2 0 for Framing Mode 3

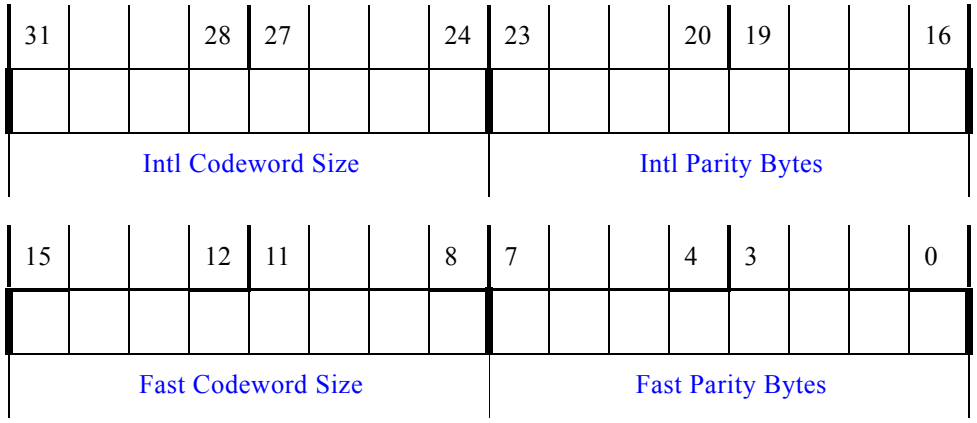

Figure 10. ATU-C/ATU-R CODE.downstream (CODE offset 0) and CODE.upstream (CODE offset 1).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

CODE returns the current codeword size and number of checkbytes for the fast and interleave paths, upstream and downstream. The formula for codeword size in either case is:

Codeword Size= symbols per codeword *[Data Bytes per frame + Overhead Bytes per frame] + Checkbytes

The Overhead bytes per frame depends on the Framing Mode and the datapath, as shown in Table 11.

Table 11 Overhead bytes per frame

	FM 0	FM 1	FM 2	FM 3
DS	3	3	1	1
US	2	2	1	1

The Data bytes per frame can be read from RATE.actual (RATE offset 0)

Notes

None.

Related CMVs

DOPT, UOPT

These CMVs set the checkbytes and symbols per codeword in Explicit-rate configuration.

RATE

RATE.actual reflects the Data bytes per frame.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

DIAG (Diagnostic)

Summary (Performance Monitoring CMVs)

Name	O	L	Access
DIAG.control **Description**: Controls the collection and reporting of diagnostic information.	0	1	NE ATU-C R/W NE ATU-R R/W
DIAG.flags **Description**: Returns the status of the defect and failure detection flags.	1	1	NE ATU-C R-only NE ATU-R R-only FE ATU-C R-only
DIAG.flags_latched **Description**: Returns the status of the latched defect and failure detection flags.	2	1	NE ATU-C R-only NE ATU-R R-only FE ATU-C R-only
DIAG.near_end_HEC_intl_anom **Description**: Returns the number of NE HEC-I anomalies that occurred during the last datapath transfer.	3	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_HEC_fast_anom **Description**: Returns the number of NE HEC-F anomalies that occurred during the last datapath transfer.	4	1	NE ATU-C R-only NE ATU-R R-only
DIAG.rx_intl_total_cell_count **Description**: Keeps count of the total number of cells received in the INTL path. This includes user, idle, unassigned, and cells with bad HEC's.	5	1	ATU-C R-only ATU-R R-only
DIAG.rx_fast_total_cell_count **Description**: Keeps count of the total number of cells received in the FAST path. This includes user, idle, unassigned, and cells with bad HEC's.	6	1	ATU-C R-only ATU-R R-only

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access
DIAG.near_end_intl_total_count **Description**: Returns the number of data cells in the Interleave Path delivered at the V-C (ATU-C) or T-R (ATU-R) interface during the last datapath transfer.	7	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_fast_total_count **Description**: Returns the number of data cells in the Fast Path delivered at the V-C (ATU-C) or T-R (ATU-R) interface during the last datapath transfer.	8	1	NE ATU-C R-only NE ATU-R R-only
DIAG.flags_1 **Description**: Reports LCD defects during the last datapath transfer.	9	1	NE ATU-C R-only NE ATU-R R-only FE ATU-C R-only
DIAG.flags_latched_1 **Description**: Reports LCD defects during the last datapath transfer.	10	1	NE ATU-C R-only NE ATU-C R-only FE ATU-C R-only
DIAG.rx_intl_idle_cell_count **Description**: Rx intl path idle cell count	11*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.rx_fast_idle_cell_count **Description**: Tx fast idle cell count	12*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.rx_intl_unassigned_cell_count **Description**: Rx intl path unassigned count	13*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.rx_fast_unassigned_cell_count **Description**: Rx fast path unassigned count	14*	1	NE ATU-C R-only NE ATU-R R-only

***Anaconda/Diamondback/Eagle Specific CMV**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access
DIAG.rx_intl_fifo_overflow **Description**: Rx intl path overflow count	15*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.rx_fast_fifo_overflow **Description**: Rx fast path overflow count	16*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.(Reserved)[]	17-21	5	
DIAG.near_end_Total_ES_Count **Description**: Returns the NE errored seconds during the last datapath transfer.	22	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Current_Attenuation **Description**: Returns the NE last measured attenuation. Reported in 1/2db steps.	23	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Previous_Attenuation **Description**: Returns the NE attenuation measured for the 10-second period prior to the 10-second period of the current attenuation. Reported in 1/2db steps.	24	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Current_SNR_Margin **Description**: Returns the NE last measured SNR margin.	25	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Previous_SNR_Margin **Description**: Returns the NE SNR margin measured for the 10-second period prior to the 10-second period of the current SNR margin.	26	1	NE ATU-C R-only
DIAG.half_db_step_near_end_current_snr _margin	27	1	NE ATU-C R-only NE ATU-R R-only

***Anaconda/Diamondback/Eagle Specific CMV**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access
DIAG.half_db_step_near_end_prvious_snr _margin	28	1	NE ATU-C R-only
DIAG.half_db_step_far_end_current_snr _margin	29	1	FE ATU-C R-only FE ATU-R R-only
DIAG.half_db_step_far_end_previous_snr _margin	30	1	FE ATU-C R-only
DIAG. (Reserved)	31	1	
DIAG._near_end_fcrc_uncorrected_blocks **Description**: Number of NE Received blocks containing uncorrected errors in the Fast path since the beginning of the link	32*	1	NE ATU-C R-only NE ATU-R R-only
DIAG._near_end_icrc_uncorrected_blocks **Description**: Number of NE Received blocks containing uncorrected errors in the Intl path since the beginning of the link	33*	1	NE ATU-C R-only NE ATU-R R-only
DIAG._near_end_good_blocks **Description**: Number of NE Received good blocks since the beginning of the link	34*		NE ATU-C R-only NE ATU-R R-only
DIAG.tx_intl_total_cell_count **Description**: Returns the number of data cells in the interleave path transmitted to the V-C (ATU-C) or RT (ATU-R) interface	35*	1	ATU-C ATU-R
DIAG.tx_fast_total_cell_count **Description**: Returns the number of data cells in the fast path transmitted to the V-C (ATU-C) or RT (ATU-R) interface	36*	1	ATU-C ATU-R
DIAG.tx_int_idle_cell_count **Description**: Tx intl latency path idle cell count*	37*	1	NE ATU-C R-only NE ATU-R R-only

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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access
DIAG.tx_intl_total_cell_count **Description**: Tx fast path idle cell count*	38*	1	NE ATU-C R-only NE ATU-R R-only
DIAG.tx_intl_total_cell_count **Description**: Returns the number of short cells transmitted in the inleave path	39*	1	ATU-C ATU-R
DIAG.tx_fast_short_cell_count **Description**: Returns the number of short cells transmitted in the fast path	40*	1	ATU-C ATU-R
DIAG.regular_bitswap_msg_count **Description**: Returns the count of regular bitswap messages received.	41	1	ATU-C R-only ATU-R R-only
DIAG. extended_bitswap_msg_count **Description**: Returns the count of extended bitswap messages received.	42	1	ATU-C R-only ATU-R R-only
DIAG. utc_msg_count **Description**: Returns the count of UTC messages received.	43	1	ATU-C R-only ATU-R R-only
DIAG.ds_bitswap_count **Description**: Returns the count of downstream bitswaps performed.	44	1	ATU-C R-only ATU-R R-only
DIAG.us_bitswap_count **Description**: Returns the count of upstream bitswaps performed.	45	1	ATU-C R-only ATU-R R-only
DIAG.far_end_Total_ES_Count **Description**: Returns the FE errored seconds during the last datapath transfer.	46	1	FE ATU-C R-only

***Anaconda/Diamondback/Eagle Specific CMV**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access
DIAG.far_end_Current_Attenuation **Description**: Returns the FE last measured attenuation. Reported in 1/2db steps.	47	1	FE ATU-C R-only FE ATU-R R-only
DIAG.far_end_Previous_Attenuation **Description**: Returns the FE attenuation measured for the 10-second period prior to the 10-second period of the current attenuation. Reported in 1/2db steps.	48	1	FE ATU-C R-only
DIAG.far_end_Current_SNR_Margin **Description**: Returns the FE last measured SNR margin.	49	1	FE ATU-C R-only FE ATU-R R-only
DIAG.far_end_Previous_SNR_Margin **Description**: Returns the FE SNR margin measured for the 10-second period prior to the 10-second period of the current SNR margin.	50	1	FE ATU-C R-only
DIAG.near_end_Rcvd_Blocks **Description**: Returns the total number of blocks received by the NE since the beginning of the link.	51	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Xmitted_Blocks **Description**: Returns the total number of blocks transmitted by the NE since the beginning of the link.	52	1	NE ATU-C R-only NE ATU-R R-only
DIAG.near_end_Corrected_Blocks **Description**: Returns the number of NE received blocks containing corrected errors since the beginning of the link.	53	1	NE ATU-C R-only NE ATU-R R-only

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Name	O	L	Access
DIAG.near_end_Uncorr_Blocks **Description**: Returns the number of NE received blocks containing uncorrectable errors since the beginning of the link.	54	1	NE ATU-C R-only NE ATU-R R-only
DIAG.far_end_Rcvd_Blocks **Description**: Returns the total number of blocks received by the FE since the beginning of the link.	55	1	FE ATU-C R-only
DIAG.far_end_Xmitted_Blocks **Description**: Returns the total number of blocks transmitted by the FE since the beginning of the link.	56	1	FE ATU-C R-only
DIAG.far_end_Corrected_Blocks **Description**: Returns the number of FE received blocks containing corrected errors since the beginning of the link.	57	1	FE ATU-C R-only
DIAG.far_end_Uncorr_Blocks **Description**: Returns the number of FE received blocks containing uncorrectable errors since the beginning of the link.	58	1	FE ATU-C R-only
DIAG.tx_intl_long_cell_count **Description**: Returns the number of long cells transmitted in the Intl path	59*	1	ATU-C ATU-R

***Anaconda/Diamondback/Eagle Specific CMV**

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Name	O	L	Access
DIAG.tx_fast_long_cell_count **Description**: Returns the number of long cells transmitted in the Fast path	60*	1	ATU-C ATU-R

***Anaconda/Diamondback/Eagle Specific CMV**

NOTE:

Not all DIAG CMVs listed in this summary have individual page descriptors that follow. The following page will describe the general DIAG.CMV bit assignment convention. DIAG CMVs that do not follow this convention have their own page descriptor in this section.

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Table 12. DIAG.name (offset 00)

Name	O	L	Access
DIAG.name **Description:** Keeps count of the total number of cells received in the Intl path. This includes user, idle, unassigned, and cells with bad HEC's	00	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	DIAG.name	Bit assignment

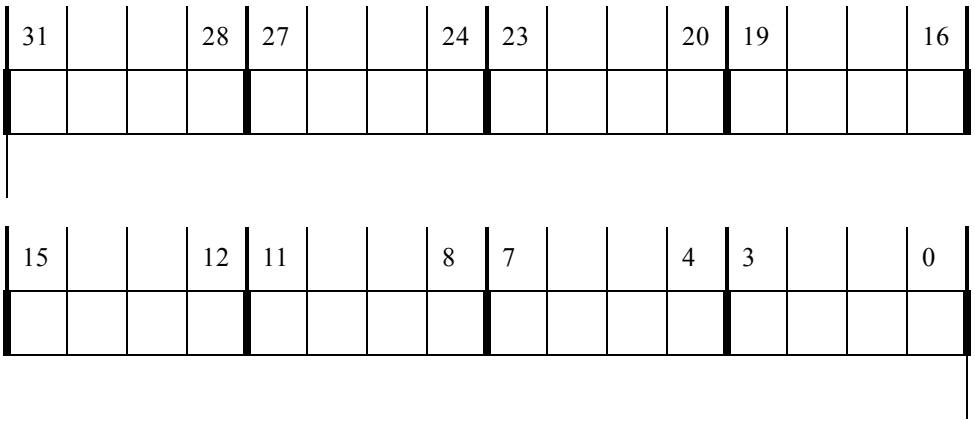

Figure 11. DIAG.name (offset 00)

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Table 13 DIAG.control (offset 0)

Bit	Name	Description
0	Clear NE Counts	1- Clear the NE 15-minute and 1-day counts. 0- Do not clear. (Default)
1	Clear FE Counts	1- Clear the FE 15-minute and 1-day counts. 0- Do not clear. (Default)
2	Clear NE Latch	1- Clear the NE latched flags (DIAG.flags_latched) 0- Do not clear. (Default)
3	Clear FE Latch	1- Clear the FE latched flags (DIAG.flags_latched) 0- Do not clear. (Default)
4	Enable LPR	1- Enable LPR diagnostics. 0- Do not enable. (Default)
5	CRC Count Selection	1- Count CRC errors only in the datapath. 0- Count all fast- and interleave-path CRC errors. (Default)
6	FE Error Processing	1- Count FE errors only if there are no NE CRC errors. 0- Count all FE errors. (Default)
15:14	Indicator Bits	These bit values get transmitted to the other ATU. They are not defined when the AD20MSP918 is running in ATM mode. Default: 0x0
16	DS Corrupt CRC Control	1- Let the ATU-C transmit corrupt CRCs. 0- Let operation be normal. NOTES: 1. Read "Usage" under "DIAG.control" on the setting and clearing of Bits 16 and 17. 2. This bit is meaningful at the ATU-C only.
17	US Corrupt CRC Control	1- Let the ATU-R transmit corrupt CRCs. 0- Let operation be normal. NOTE: This bit is meaningful at the ATU-C only.

Further bit descriptions for DIAG.control (offset 0)

DIAG.control (DIAG offset 0)

DIAG.control controls the available diagnostics information and performs other simple diagnostics functions. Here are notes on some of the bits:

Bit 4

Allows the ME to enable loss-of-power (LPR) diagnostics. The ME must indicate a LPR condition by enabling the IRQL0 interrupt on the ADSP2183 microprocessor. For proper processing, the interrupt must be held low (active) for the duration of the LPR event.

If the ME has set bit 4, the ATU will handle near-end and far-end LPR diagnostic processing as defined in *[1]*, including transmission of "Dying Gasp" EOC messages from the ATU-R to the ATU-C. If the ME has not set bit 4, the ATU will ignore the IRQL0 interrupt and will not process "Dying Gasp" EOC messages.

NOTE: LPR failure indicators may occur up to 0.5 seconds after the corresponding LOS failure.

Bit 5

When the modem uses coding (see ADPT.downstream), the path that it has selected for data, due to coding gain, will have a higher margin than the other path. If the modem is using both fast and interleave path errors to calculate the CRC errored second count, the path with the lower margin may dominate the count, even though the user is generally interested only in datapath errors.

You can control this circumstance by using Bit 5 of DIAG.control to select the type of CRC error affecting the CRC errored second count CMVs. By setting this bit, the ME can command the modem to ignore any errors that do not occur on the datapath.

For example, if the ME sets bit 5 and then initiates a rate-adaptive link that uses Interleave Path, the software will count only interleave-path CRC errors. This feature allows the ME to account for any differences between fast-path margin and interleave-path margin (refer to OPTN for further details).

Bit 6

Allows the ME to configure how far-end error flags are processed. If the bit is set, the modem will assume that the far-end indicator bits are in error if a near-end CRC is received and will therefore ignore them. If Bit 6 is cleared (the default), the modem will process all far-end indicator bits, even if near-end CRC errors are present.

Bits 15:14

You can use bits 14 and 15 to transmit indicator information from one ATU to the other, as defined in *[1]*. For example, if the ME-C sets them in DIAG.control, the ATU-C will send this information over the datapath during subsequent superframes, until the ME-C clears bits 14

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and 15. The ATU-R will report these indicators as far-end flags in DIAG.flags and DIAG.flags_latched CMVs. This function is bidirectional (US or DS) and can be used to transfer external indicators from ME to ME.

Bits 17:16

When the ME-C sets DIAG.control bit 16, the ATU-C sends a "Request corrupt CRC" EOC message to the ATU-R. When the ME-C sets DIAG.control bit 17, the ATU-C sends a "Notify corrupt CRC" EOC message to the ATU-R.

Only one EOC message gets sent at a time. therefore, if you have the ME-C write 1 to bits 16 and 17 in the same DIAG.control (Offset 0) message, you will not be able to generate corrupt CRCs on both downstream and upstream.

The best way to generate corrupt CRCs on both DS and US is to set bit 17 first (to generate US corrupt CRCs), then set bit 16 (to generate DS corrupt CRCs). Examples:

0x00020000 (generates US CRC errors)

0x00030000 (generates DS CRC errors)

The same rule applies to clearing the corrupt CRCs on both DS and US. First clear bit 17 (to stop US corrupt CRCs) then clear bit 16 (to stop DS corrupt CRCs). Examples:

0x00010000 (clears US CRC errors)

0x00000000 (clears DS CRC errors)

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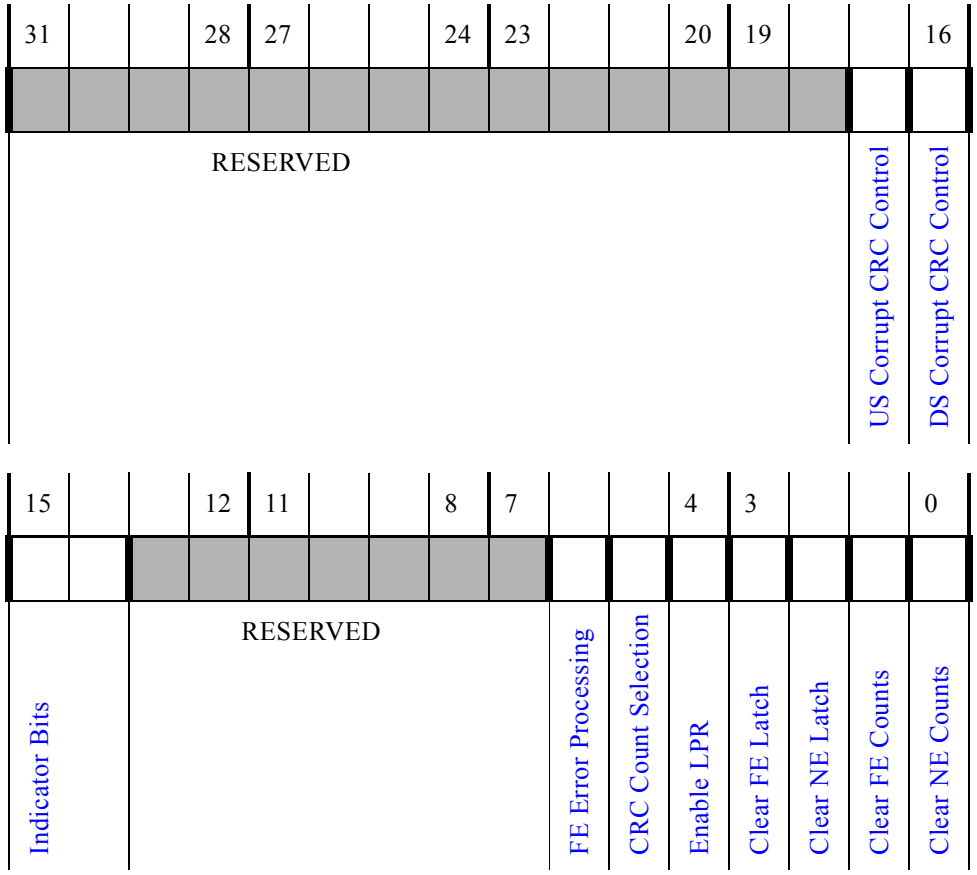

Figure 12. DIAG.control (offset 0)

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31			28	27			24	23			20	19			16
FE Fast HEC Failure	FE Intl HEC Failure	FE Fast LOD Anomaly	FE Intl LOD Anomaly	RESERVED	RESERVED	FE LPR Failure	FE LPR Defect	FE SEF Failure (LOF)	FE SEF Defect	FE LOS Failure	FE LOS Defect	FE Intl CRC	FE Fast CRC	FE Intl FEC	FE Fast FEC

15			12	11			8	7			4	3			0
NE Fast HEC Failure	NE Intl HEC Failure	NE Fast LOD Anomaly	NE Intl LOD Anomaly	RESERVED	RESERVED	NE LPR Failure	NE LPR Defect	NE SEF Failure (LOF)	NE SEF Defect	NE LOS Failure	NE LOS Defect	NE Intl CRC	NE Fast CRC	NE Intl FEC	NE Fast FEC

Figure 13. DIAG.flags (DIAG offset 1), DIAG.flags_latched (DIAG offset 2).

Table 13 and Table 6-14 list the bit meanings of a DIAG.flags or a DIAG.flags_latched. The tables include only the “set” meanings. For example, if “set” means “There was an NE LPR Failure”, then “clear” would mean “There was no NE LPR Failure.”

Table 14 DIAG.flags (DIAG offset 1), DIAG.flags_latched (offset 2)

Bit	Name	Value When Set
0	NE Fast FEC	There was NE fast-path FEC correction in the preceding superframe.
1	NE Intl FEC	There was NE interleave-path FEC correction in the preceding superframe.
2	NE Fast CRC	There was a fast-path CRC error in the preceding superframe.
3	NE Intl CRC	There was an NE interleave-path CRC error in the preceding superframe.
4	NE LOS Defect	There was an NE LOS defect.
5	NE LOS Failure	There was an NE LOS failure.
6	NE SEF Defect	There was an NE SEF defect.
7	NE SEF Failure (LOF)	There was an NE SEF failure.
8	NE LPR Defect	There was an NE LPR defect.
9	NE LPR Failure	There was an NE LPR failure.
12	NE Intl LOD Anomaly	There was an NE interleave-path LOD (Loss of Delineation) error.
13	NE Fast LOD Anomaly	There was an NE fast-path LOD error.
14	NE Intl HEC Failure	There was an NE interleave-path HEC (Header Error Control) error.
15	NE Fast HEC Failure	There was an NE fast-path HEC error.
16	FE Fast FEC	There was FE fast-path FEC correction in the preceding superframe.

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Table 14 DIAG.flags (DIAG offset 1), DIAG.flags_latched (offset 2)

Bit	Name	Value When Set
17	FE Intl FEC	There was FE interleave-path FEC correction in the preceding superframe.
18	FE Fast CRC	There was an FE fast-path CRC error in the preceding superframe.
19	FE Intl CRC	There was an FE interleave-path CRC error in the preceding superframe.
20	FE LOS Defect	There was an FE LOS defect.
21	FE LOS Failure	There was an FE LOS failure.
22	FE SEF Defect	There was an FE SEF defect.
23	FE SEF Failure (LOF)	There was an FE SEF Failure.
24	FE LPR Defect	There was an FE LPR defect.
25	FE LPR Failure	There was an FE LPR failure.
28	FE Intl LOD Anomaly	There was an FE interleave-path LOD error.
29	FE Fast LOD Anomaly	There was an FE fast-path LOD error.
30	FE Intl HEC Failure	There was an FE interleave-path HEC error.
31	FE Fast HEC Failure	There was an FE fast-path HEC error.

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Usage

DIAG provides performance-monitoring information.

Table 15 DIAG.rx_intl_total_cell_count (offset 5)

Name	O	L	Access
DIAG.rx_intl_total_cell_count **Description:** Keeps count of the total number of cells received in the Intl path. This includes user, idle, unassigned, and cells with bad HEC's	5	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_intl_total_cell_count	

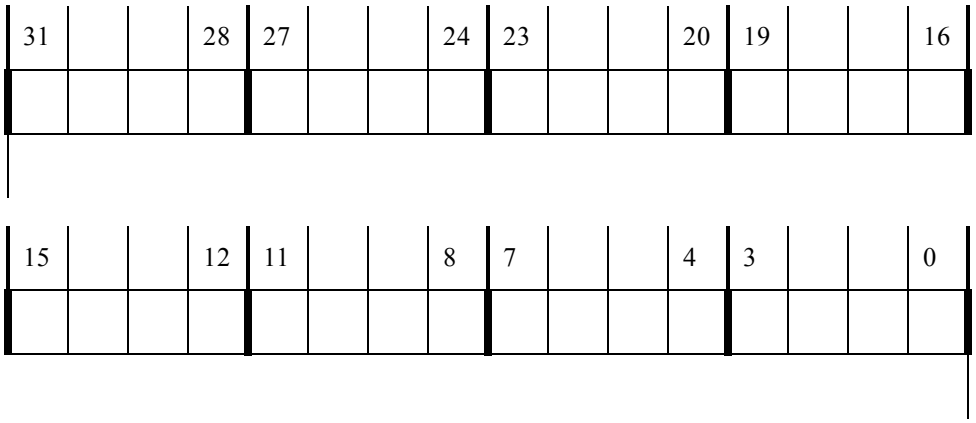

Figure 14. DIAG.rx_intl_total_cell_count (offset 5)

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Table 16 DIAG.rx_fast_total_cell_count (offset 6)

Name	O	L	Access
DIAG.rx_fast_total_cell_count **Description:** Keeps count of the total number of cells received in the Fast path. This includes user, idle, unassigned, and cells with bad HEC's	6	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_fast_total_cell_count	

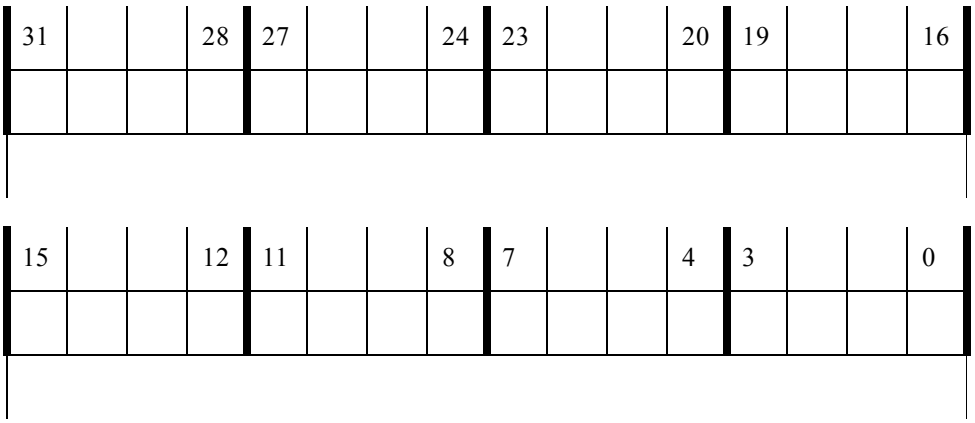

Figure 15. DIAG.rx_fast_total_cell_count (offset 6)

Table 14 and Table 15 list the bit meanings of a DIAG.flags_1 or a DIAG.flags_latched_1. The tables include only the “set” meanings. For example, if “set” means “There was a NE LCD Defect”, then “clear” would mean “There was no NE LCD Defect.”

Table 17 DIAG.flags_1 (DIAG offset 9), DIAG.flags_latched_1 (DIAG offset 10)

Bit	Name	Value When Set
0	NE OCD-I	There was a Near End OCD anomaly in the Interleave Path.
1	NE OCD-F	There was a Near End OCD anomaly in the Fast Path.
4	NE LCD-I	There was a Near End LCD anomaly in the Interleave Path.
5	NE LCD-F	There was a Near End LCD anomaly in the Fast Path.
6	NE NCD-I	There was a Near End NCD anomaly in the Interleave Path.
7	NE NCD-F	There was a Near End NCD anomaly in the Fast Path.
12	NE LCD-I	There was a Near End LCD failure in the Interleave Path.
13	NE LCD-F	There was a Near End LCD failure in the Fast Path.
14	NE NCD-I	There was a Near End NCD failure in the Interleave Path.
15	NE NCD-F	There was a Near End NCD failure in the Fast Path.
16	FE OCD-I	There was a Far End OCD anomaly in the Interleave Path.

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Table 17 DIAG.flags_1 (DIAG offset 9), DIAG.flags_latched_1 (DIAG offset 10)

Bit	Name	Value When Set
17	FE OCD-F	There was a Far End OCD anomaly in the Fast Path.
20	FE LCD-I	There was a Far End LCD anomaly in the Interleave Path.
21	FE LCD-F	There was a Far End LCD anomaly in the Fast Path.
22	FE NCD-I	There was a Far End NCD anomaly in the Interleave Path.
23	FE NCD-F	There was a Far End NCD anomaly in the Fast Path.
28	FE LCD-I	There was a Far End LCD failure in the Interleave Path.
29	FE LCD-F	There was a Far End LCD failure in the Fast Path.
30	FE NCD-I	There was a Far End NCD failure in the Interleave Path.
31	FE NCD-F	There was a Far End NCD failure in the Fast Path.

DIAG.flags (DIAG offsets 1,9), DIAG.flags_latched (DIAG offsets 2,10)

Indicator bits 28 through 31 (i.e., far-end bits 12 through 15) report the status of ATM indicator bits as set by the far-end ATU. The far-end ATM indicator bits are currently the only far-end indicators available at the ATU-R.

Margin and Attenuation CMVs

Margin is given in integer dB. Attenuation is given in dB in 15.1 notation. On the ATU-R side, the minimum attenuation reported is 9 dB (0x12 in 15.1 notation).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Notes

1. The ME can configure the ATU-R and ATU-C to trigger the PF4 line based on some of the diagnostics events above, using the FLAG CMV (refer to FLAG).
2. DIAG offsets 3-8 reset to zero on a reset of the chipset.

Related CMVs

FLAG

Sets events that will trigger a signal on the PF4 line. You can use DIAG to discover these events.

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31			28	27			24	23			20	19			16
FE NCD-F	FE NCD-I	FE LCD-F	FE LCD-I	Reserved				FE NCD-F	FE NCD-I	FE LCD-F	FE LCD-I	Reserved	Reserved	FE OCD-F	FE OCD-I

15			12	11			8	7			4	3			0
NE NCD-F	NE NCD-I	NE LCD-F	NE LCD-I	Reserved				NE NCD-F	NE NCD-I	NE LCD-F	NE LCD-I	Reserved	Reserved	NE OCD-F	NE OCD-I

Figure 16. DIAG.flags_1 (DIAG offset 9), DIAG.flags_latched_1 (DIAG offset 10).

Usage

DIAG provides performance-monitoring information.

Table 18 DIAG.rx_intl_total_cell_count (offset 5)

Name	O	L	Access
DIAG.rx_intl_total_cell_count **Description:** Keeps count of the total number of cells received in the Intl path. This includes user, idle, unassigned, and cells with bad HEC's	5	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_intl_total_cell_count	

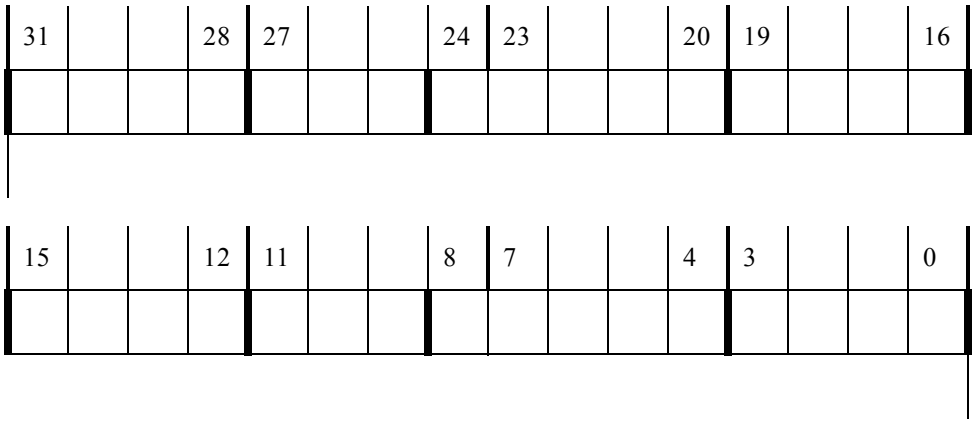

Figure 17. DIAG.rx_intl_total_cell_count (offset 5)

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Table 19 DIAG.rx_fast_total_cell_count (offset 6)

Name	O	L	Access
DIAG.rx_fast_total_cell_count **Description:** Keeps count of the total number of cells received in the Fast path. This includes user, idle, unassigned, and cells with bad HEC's	6	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_fast_total_cell_count	

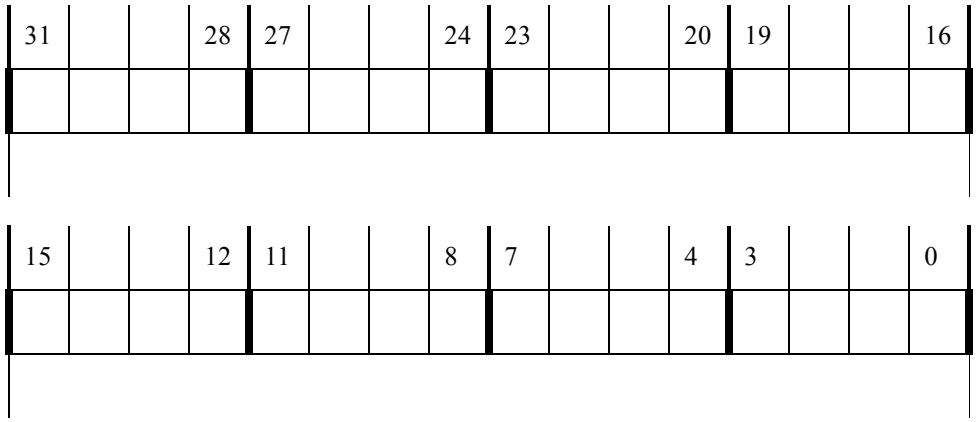


Figure 18. DIAG.rx_fast_total_cell_count (offset 6)

Table 20 DIAG.rx_intl_idle_cell_count (offset 11)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_intl_idle_cell_count **Description:** This keeps a count of the number of idle cells in the intl latency path that are detected while in the ATM Sync State and subsequently discarded. Idle cells are always discarded at the receiver.	11	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_intl_idle_cell_count	Rx intl path idle cell count

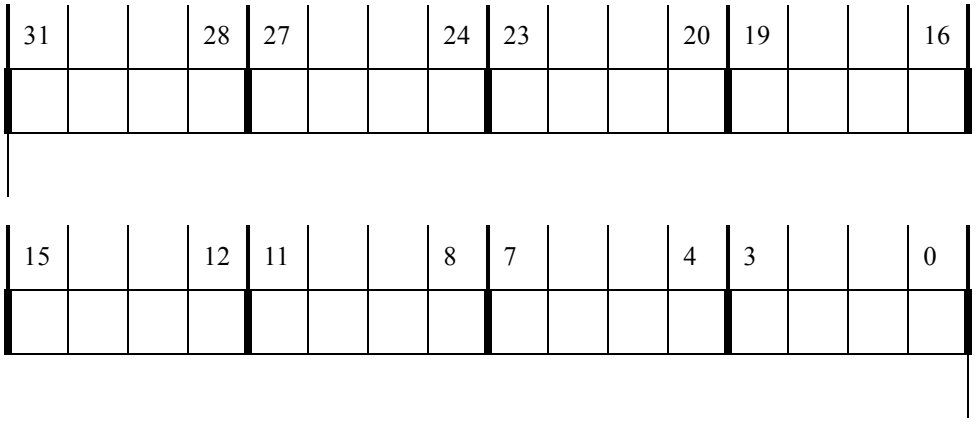


Figure 19. DIAG.rx_intl_idle_cell_count (offset 11)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 21 DIAG.rx_fast_idle_cell_count (offset 12)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_fast_idle_cell_count **Description:** This keeps a count of the number of idle cells in the fast latency path that are detected while in the ATM sync state and subsequently discarded. Idle cells are always discarded at the receiver.	12	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_fast_idle_cell_count	Rx Fast path idle cell count

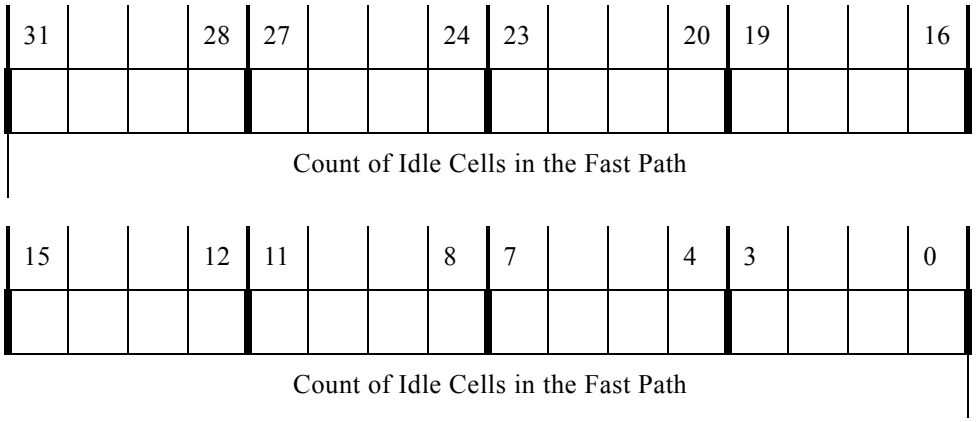


Figure 20. DIAG.rx_fast_idle_cell_count (offset 12)

Table 22 DIAG.rx_intl_unassigned_cell_count (offset 13)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_intl_unassigned_cell_count **Description:** This keeps a count of the number of unassigned cells received on the intl latency path that are detected while in the ATM Sync state. This counter increments whether or not unassigned cells are configured to be discarded (see OPTN.atm_fifo, offset 15, bit 31). If these cell types are configured NOT to be discarded, these cells will be treated as valid cells and included in the user cell count for the interleaved ADSL latency path.	13	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_intl_unassigned_cell_count	Rx Intl path unassigned count

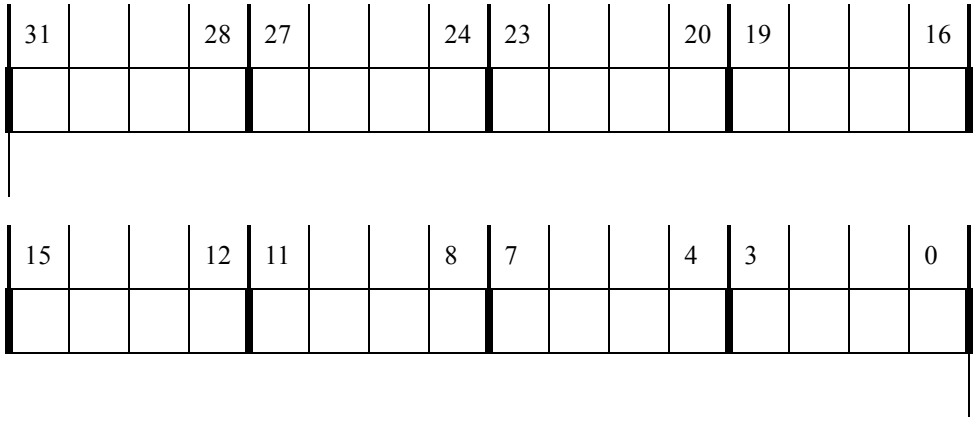


Figure 21. DIAG.rx_intl_unassigned_cell_count (offset 13)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 23 DIAG.rx_fast_unassigned_cell_count (offset 14)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_fast_unassigned_cell_count **Description:** This keeps a count of the number of unassigned cells received on the fast latency path that are detected while in the ATM Sync state. This counter increments whether or not unassigned cells are configure to be discarded (see OPTN.atm_fifo, offset 15, bit 31). If these cell types are configured NOT to be discarded, these cells will be treated as valid cells and included in the user cell count for the fast latency path.	14	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_fast_unassigned_cell_count	Rx fast path unassigned count

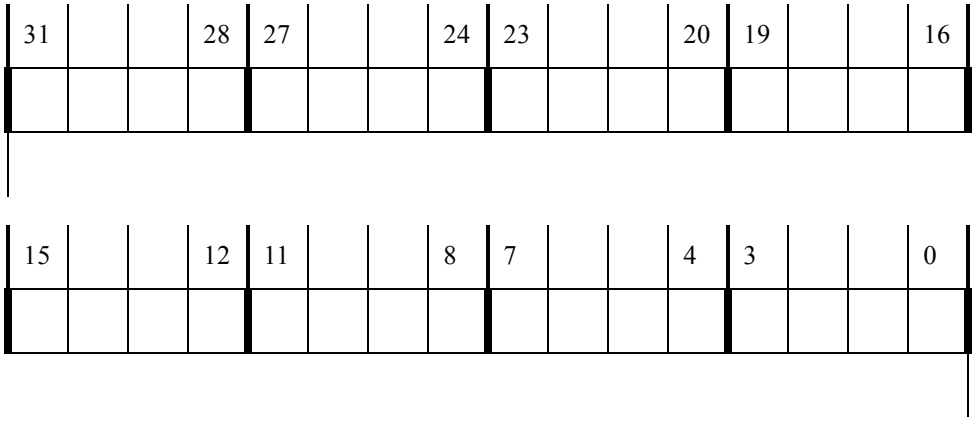


Figure 22. DIAG.rx_fast_unassigned_cell_count (offset 14)

Table 24 DIAG.rx_intl_fifo_overflow (offset 15)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_intl_fifo_overflow **Description:** This keeps a count of the number of cells received in the intl latency path and discarded because the associated Rx FIFO was full. Cells received when the associated Rx FIFO is full are always discarded.	15	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_intl_fifo_overflow	Rx intl path overflow count

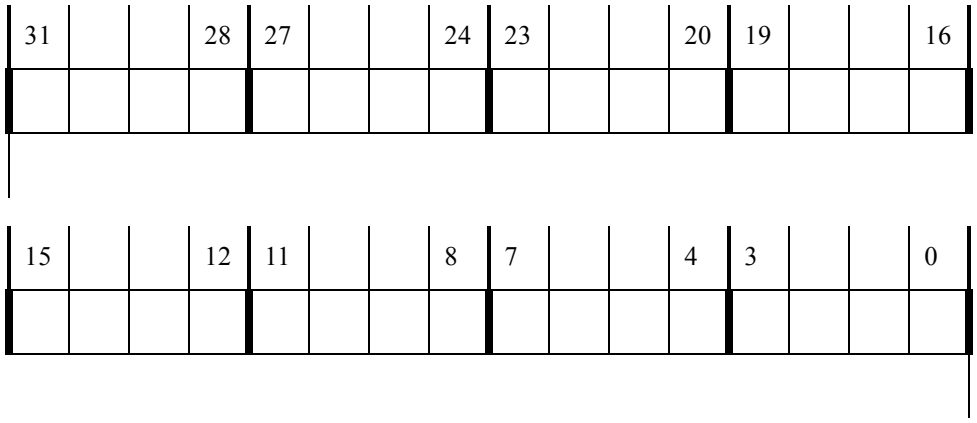


Figure 24-1. DIAG.rx_int_fifo_overflow (offset 15)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 25 DIAG.rx_fast_fifo_overflow (offset 16)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.rx_fast_fifo_overflow **Description:** This keeps a count of the number of cells received on the fast latency path and discarded because the associated Rx FIFO was full. Cells received when the associated Rx FIFO is full are always discarded.	16	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.rx_fast_fifo_overflow	Rx Fast path overflow

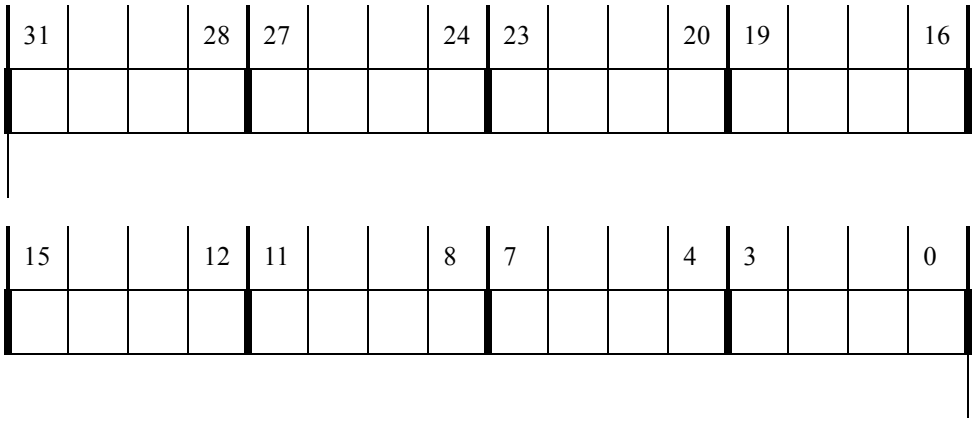


Figure 23. DIAG.rx_fast_fifo_overflow (offset 16)

Table 26 DIAG_near_end_fcrc_uncorrected_blocks (offset 32)

Name	O	L	Access
DIAG._near_end_fcrc_uncorrected_blocks **Description**: Number of NE Received blocks containing uncorrected errors in the Fast path since the beginning of the link	32	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG_near_end_fcrc-uncorrected_blocks	

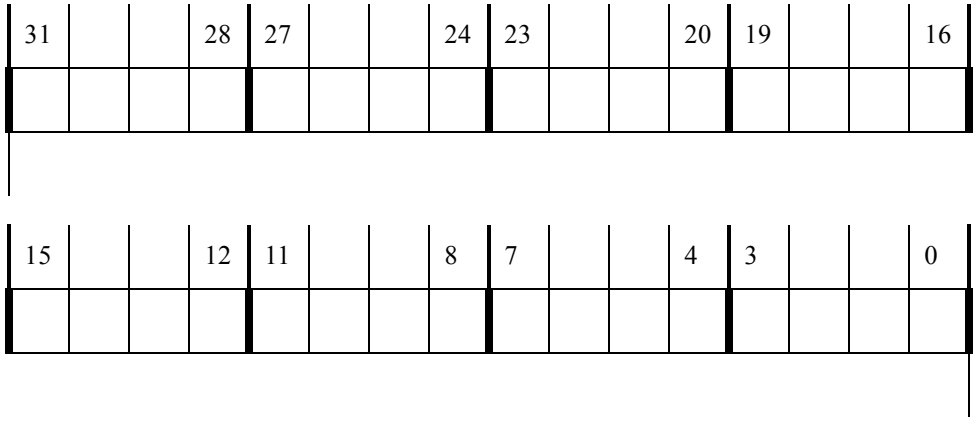


Figure 24. DIAG_near_end_fcrc-uncorrected_blocks (offset 32)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 27 DIAG_near_end_icrc_uncorrected_blocks (offset 33)

Name	O	L	Access
DIAG._near_end_fcrc_uncorrected_blocks **Description**: Number of NE Received blocks containing uncorrected errors in the Intl path since the beginning of the link	33	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG_near_end_icrc_uncorrected_blocks	

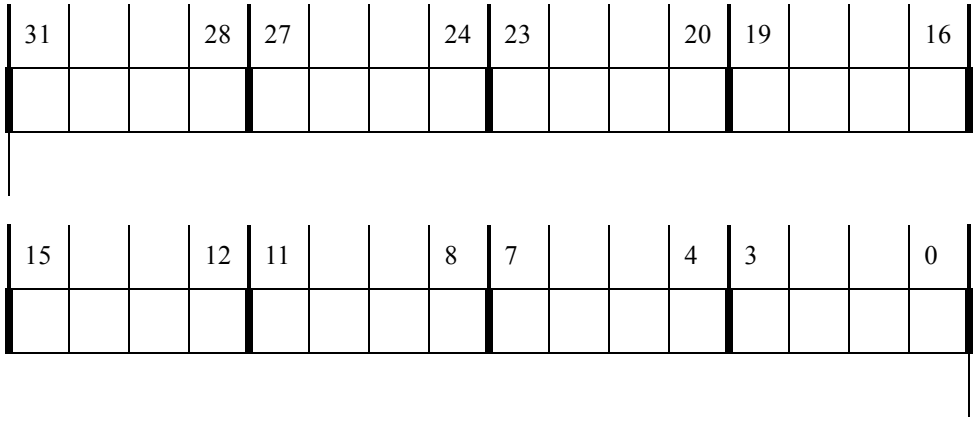


Figure 25. DIAG_near_end_icrc_uncorrected_blocks (offset 33)

Table 28 DIAG_near_end_good_blocks (offset 34)

Name	O	L	Access
DIAG._near_end_good_blocks **Description**: Number of NE Received blocks containing uncorrected errors in the Intl path since the beginning of the link	34	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG_near_end_good_blocks	

31			28	27			24	23			20	19			16

15			12	11			8	7			4	3			0

Figure 26. DIAG_near_end_good_blocks (offset 34)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 70. DIAG.tx_intl_total_cell_count (offset 35)

Name	O	L	Access
DIAG.tx_intl_total_cell_count **Description:** Returns the number of data cells in the interleave path transmitted to the V-C (ATU-C) or RT (ATU-R) interface	35	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_intl_total_cell_count	Returns the number of data cells in the interleave path transmitted to the V-C (ATU-C) or RT (ATU-R) interface

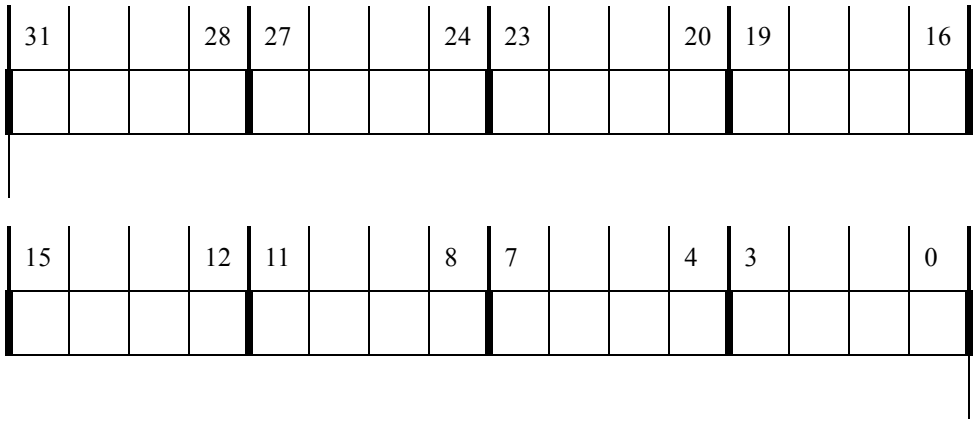


Figure 27. DIAG.tx_intl_total_cell_count (offset 35)

Table 71. DIAG.tx_fast_total_cell_count (offset 36)

Name	O	L	Access
DIAG.tx_fast_total_cell_count **Description:** Returns the number of data cells in the fast path transmitted to the V-C (ATU-C) or RT (ATU-R) interface	36	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_fast_total_cell_count	Returns the number of data cells in the fast path transmitted to the V-C (ATU-C) or RT (ATU-R) interface

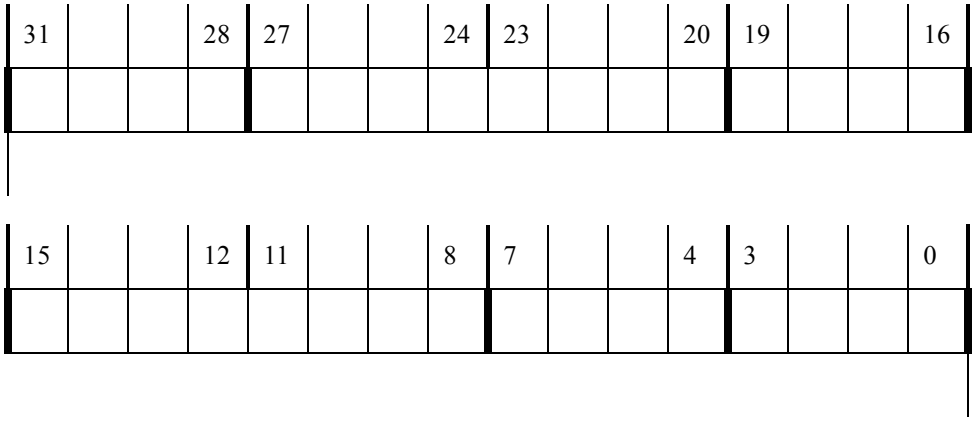


Figure 28. DIAG.tx_fast_total_cell_count (offset 36)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 72. DIAG.tx_intl_idle_cell_count (offset 37)

Name	O	L	Access
DIAG.tx_intl_idle_cell_count **Description:** This keeps a count of the total number of idle cells generated on the intl latency path.	37	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.tx_intl_idle_cell_count	Tx intl latency path Idle cell count

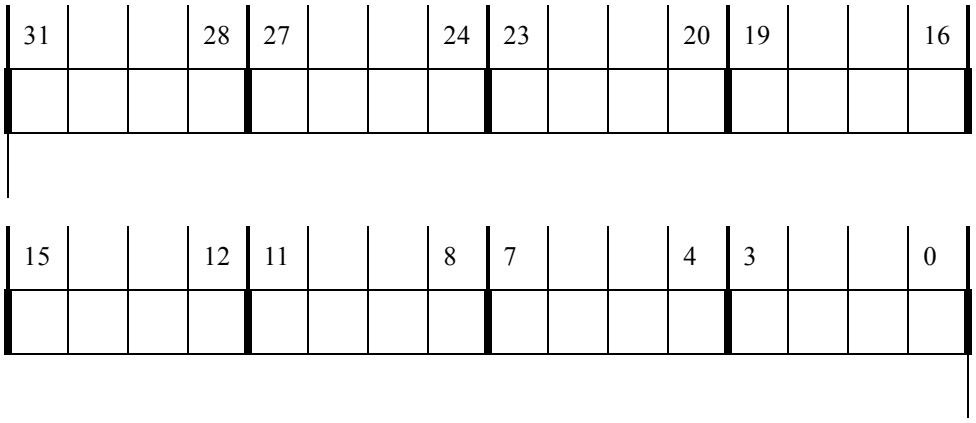


Figure 29. DIAG.tx_intl_idle_cell_count (offset 37)

Table 73. DIAG.tx_fast_idle_cell_count (offset 38)

Name	O	L	Access
DIAG.tx_fast_idle_cell_count **Description:** This keeps a count of the total number of idle cells generated on the fast latency path.	38	1	NE ATU-C R-only NE ATU-R R-only

Bits	Name	Description
31:0	DIAG.tx_fast_idle_cell_count	Tx fast path Idle cell count

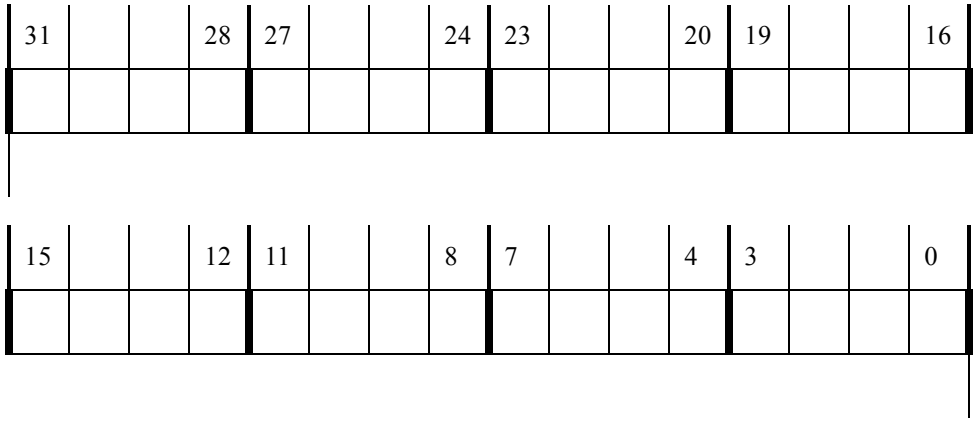


Figure 30. DIAG.tx_fast_idle_cell_count (offset 38)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 74 DIAG.tx_intl_short_cell _count (offset 39)

Name	O	L	Access
DIAG.tx_intl_short_cell_count **Description:** Returns the number of short cells transmitted in the interleave path.	39	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_intl_short_cell_count	Returns the number of short cells transmitted in the interleave path.

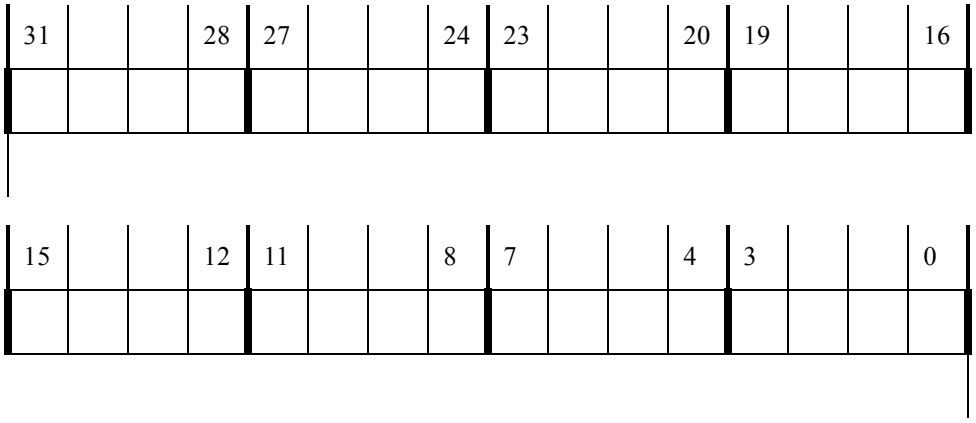


Figure 31. DIAG.tx_intl_short_cell_count (offset 39)

Table 75. DIAG.tx_fast_short_cell_count (offset 40)

Name	O	L	Access
DIAG.tx_fast_short_cell_count **Description:** Returns the number of short cells transmitted in the fast path.	40	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_fast_short_cell_count	Returns the number of short cells transmitted in the fast path.

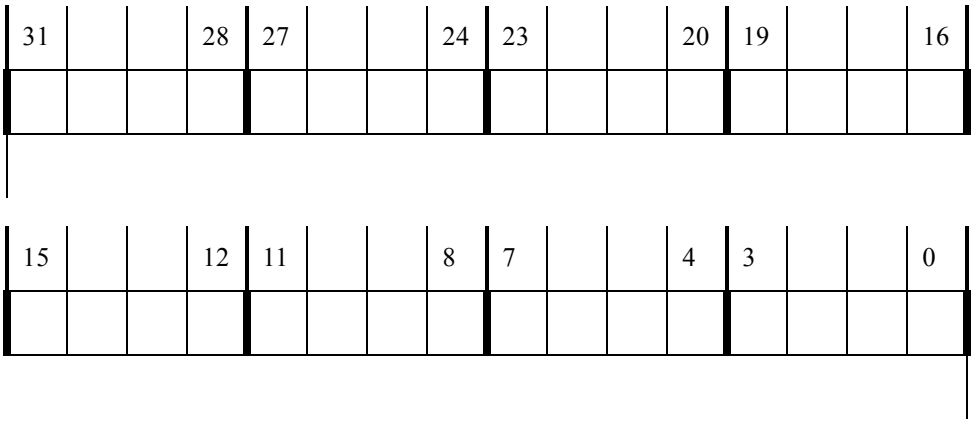


Figure 32. DIAG.tx_fast_short_cell_count (offset 40)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 29 DIAG.tx_intl_long_cell_count (offset 59)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.tx_intl_long_cell_count **Description:** Returns the number of long cells transmitted in the intl path.	59	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_intl_long_cell_count	Returns the number of long cells transmitted in the intl path.

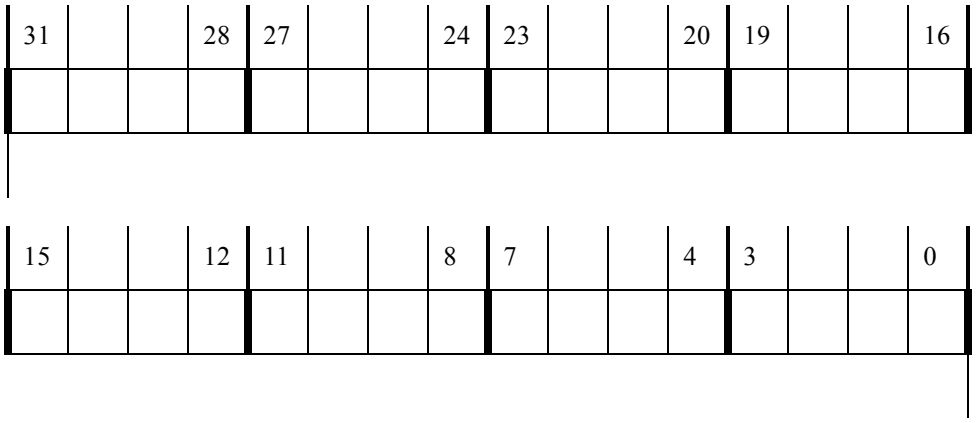


Figure 33. DIAG.tx_intl_long_cell_count (offset 59)

Table 30 DIAG.tx_fast_long_cell_count (offset 60)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
DIAG.tx_fast_long_cell_count **Description:** Returns the number of long cells transmitted in the fast path.	60	1	ATU-C ATU-R

Bits	Name	Description
31:0	DIAG.tx_fast_long_cell_count	Returns the number of long cells transmitted in the fast path.

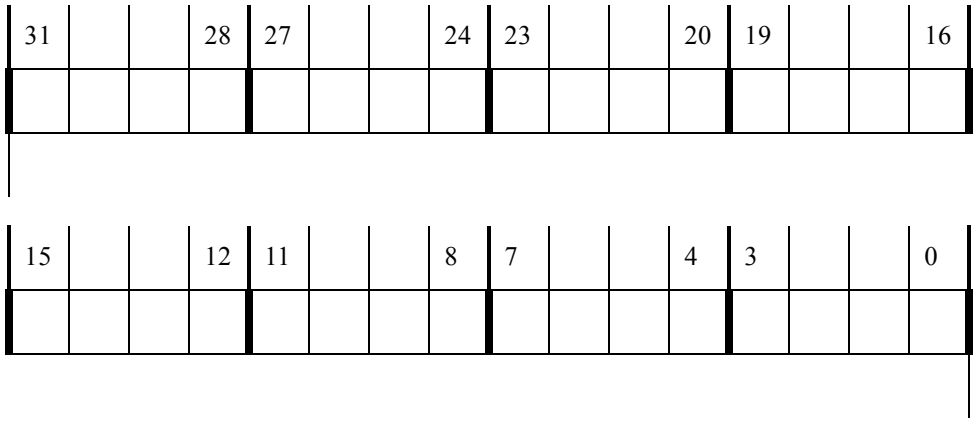


Figure 34. DIAG.tx_fast_long_cell_count (offset 60)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

DOPT

Downstream Options for Explicit Rate Configuration

Summary

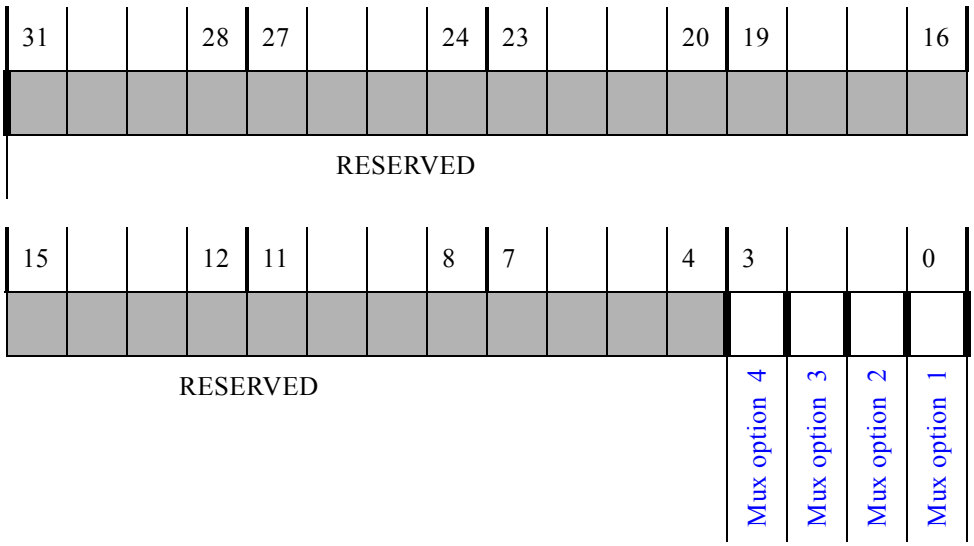
Name	O	L	Access	Description
DOPT.mux_option	0	1	ATU-C R/W	Specifies Interleave Path or Fast Path for 4 options.
DOPT.simplex_bytes	1	1	ATU-C R/W	Specifies downstream data rates in Simplex path (AS) for 4 options.
DOPT.duplex_bytes	2	1	ATU-C R/W	Specifies downstream data rates in Duplex path (LS) for 4 options.
DOPT.fast_check_bytes	3	1	ATU-C R/W	Specifies number of Fast path checkbytes for 4 options.
DOPT.intl_check_bytes	4	1	ATU-C R/W	Specifies number of Inter-leave path checkbytes for 4 options.
DOPT.intl_depth	5	1	ATU-C R/W	Specifies Interleave depth for 4 options.
DOPT.symbols_per_codeword	6	1	ATU-C R/W	Specifies number of symbols per codeword for 4 options.
DOPT.required_margin	7	1	ATU-C R/W	Specifies the required SNR margin.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 31 DOPT.mux_option (offset 0)

Bit	Name	Description
0	Mux Option 1	0 -Use Fast Path in DS for Option 1 1 -Use Interleave Path in DS for Option 1
1	Mux Option 2	0 -Use Fast Path in DS for Option 2 1 -Use Interleave Path in DS for Option 2
2	Mux Option 3	0 -Use Fast Path in DS for Option 3 1 -Use Interleave Path in DS for Option 3
3	Mux Option 4	0 -Use Fast Path in DS for Option 4 1 -Use Interleave Path in DS for Option 4
31:4	RESERVED	Default: 0x0

Figure 35. DOPT.mux_option (offset 0)



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

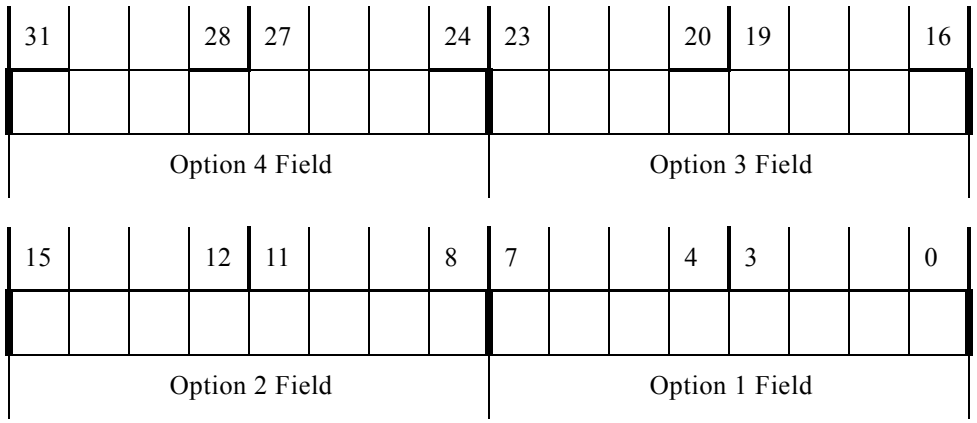


Figure 36. DOPT offsets 1-6.

The Option 1, etc., Fields contain the parameter that is appropriate to that offset for that option. For example, for DOPT.simplex_bytes, the Option 1 Field contains the DS data rate to be associated with Option 1, etc.

Table 16 below states the meanings of the option fields for the relevant CMVs.

Table 32 DOPT Option Field Values

DOPT Name	Option Field Description
DOPT.simplex_bytes (DOPT offset 1)	• Specifies the DS data rate in for the simplex path bytes per symbol for 4 options. • The rate in bits per symbol (bps) is equal to the rate in bytes per symbol multiplied by 32,000. • Rates can range from 0x01 (32 Kbps) to 0x80 (8.16 Mbps) for full-rate in multiples of 0x01. Example: Bytes per symbol = 0x0A. The data rate = 320 Kbps. Example: A DS rate of 640 Kbps is required for each option. DOPT dataword value: 0x14141414.

Table 32 DOPT Option Field Values

DOPT Name	Option Field Description
DOPT.duplex_bytes (DOPT offset 2)	• Specifies the DS data rate for the duplex path in bytes per Symbol for 4 options.
DOPT.fast_check_bytes (DOPT offset 3)	• Specifies the number of checkbytes, in bytes/codeword, on fast-path data. • The values in this word are only valid for Fast Path (DOPT.mux_option) and should be cleared otherwise. • Each possible value must be a multiple of the number of symbols per codeword (DOPT.symbols_per_codeword). • Each value must be even and <= 0x14.
DOPT.intl_check_bytes (DOPT offset 4)	• Specifies the number of checkbytes, in bytes/codeword, on interleave-path data. • The values in this word are only valid for Interleave Path (DOPT.mux_option) and should be cleared otherwise. • Each possible value must be a multiple of the number of symbols per codeword (DOPT.symbols_per_codeword). • Each value must be even and <= 0x14.
DOPT.intl_depth (DOPT offset 5)	• Specifies interleave depth, in bytes (i.e., the number of bytes between previously adjacent bytes after interleaving). • The values in this word are only valid for Interleave Path (DOPT.mux_option) and should be cleared otherwise. • Interleaving is only useful in combination with coding. If you don't select coding, then clear the interleave depth. • The interleave depth must be a power of 2 and < 64. • This condition must be true: **interleave depth * symbols/codeword < 255**.

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Table 32 DOPT Option Field Values

DOPT Name	Option Field Description
DOPT.symbols_per_codeword (DOPT offset 6)	• Specifies the codeword length, in symbols per codeword, for 4 options. • The multiple-frame-per-codeword feature is only available for Interleave Path. The value must be 1 for Fast Path. • The value must be a power of 2, up to a maximum of 64. • The expression **((Data Bytes + Overhead/Symbol)* (Symbols/Codeword) + Parity Bytes) <= 255** must be true, where the Overhead/Symbol is determined by the framing mode selected, as defined in *[1]*.

Table 33 DOPT.required_margin (offset 7)

Bit	Name	**Description**
7:0	Required DS Margin	This specifies the required DS margin in dB. It is the same for all four (4) options. Example, if you set this parameter is to 6, the AD20MSP918 will require the link to maintain a link margin of 6 dB, based on a target bit error rate (BER) of 1.0E-7. If this margin is not met, the link initiation will fail. The nominal value for the required margin is 6dB. This margin does not include coding gain. The margin must be less than 127 (decimal).

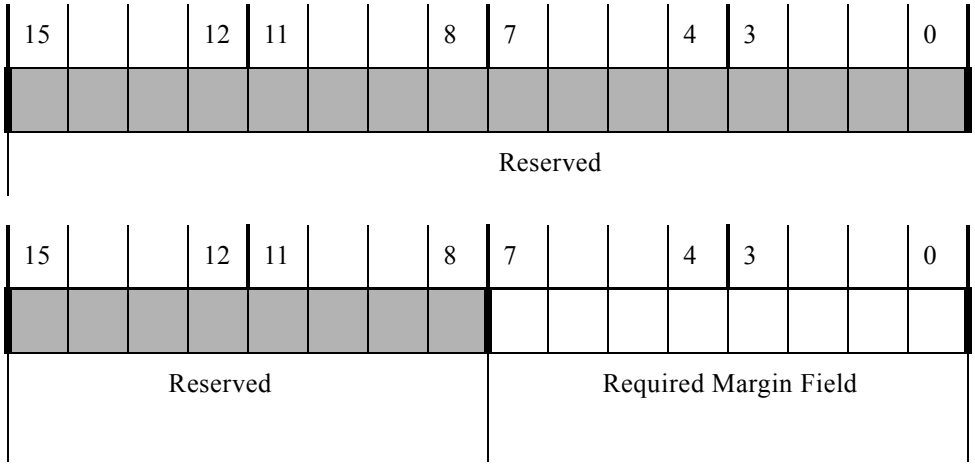

Figure 37. DOPT.required_margin (offset 7)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

DOPT sends DS configuration parameters for Explicit-rate Configuration only to the ATU-C. If the ME does not properly and completely set DOPT and UOPT, the results of the initialization will be undefined.

DOPTs and UOPTs are basically of two types: interleave-path and fast-path. The field values support one of these concepts or the other.

Interleaving spreads out the effects of burst errors prior to the error-correction stage. The purpose is to reduce the number of errors seen within any one Reed-Solomon codeword.

Recall that the number of errors within each codeword that can be corrected is no more than half the number of parity bytes. As the interleave depth is increased, burst errors become more spread out and the Reed-Solomon effectiveness increases. The cost is an increase in latency.

Increasing the frames per codeword allows lower data rates to operate with larger code-word sizes and better performance.

For more of a theoretical presentation, refer to Chapter 4.

Notes

None.

Related CMVs

UOPT

Specifies the US configuration parameters for Explicit Rate Configuration.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

FLAG

Summary

Name	O	L	Access	Description
FLAG.mask	0	1	ATU-C R/W ATU-R R/W	Sets the events on which an ATU will send an unsolicited flag signal to its ME. Default: 0x00000020

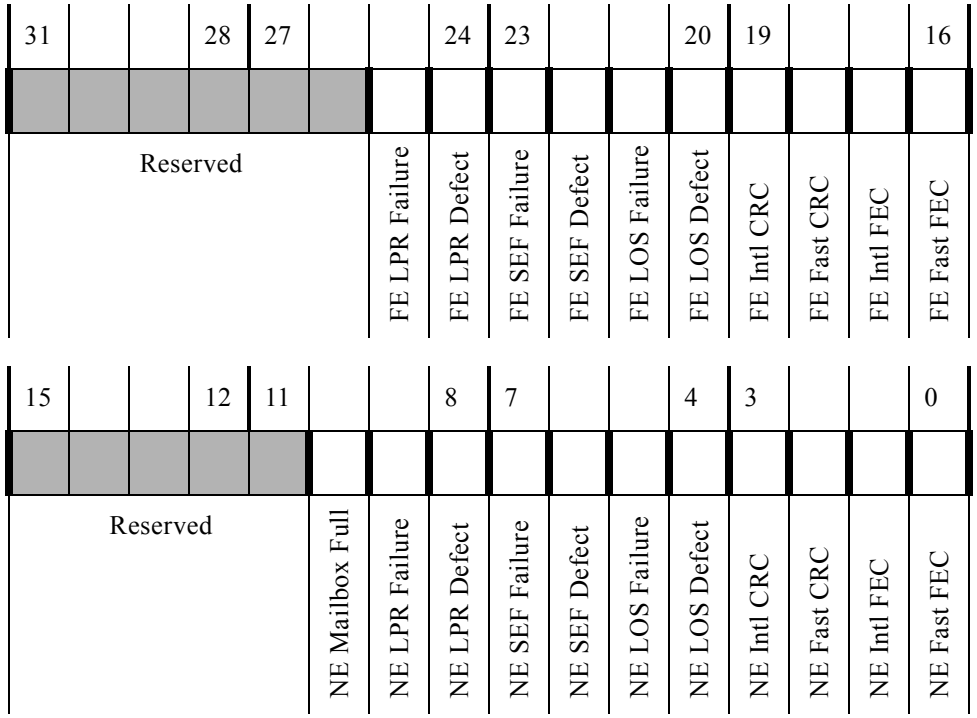

Figure 38. FLAG.mask (offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

Triggering The Flag Signal

FLAG.mask (Offset 0) programs the triggers for the Flag Signal. For example, if the ME sends a FLAG.mask with bits 0 and 1 set, and the ATU detects a near-end FEC error on the Fast or Interleave Paths, the Flag Signal will be triggered. The ME would need to use a DIAG.flags_latched (Offset 2) CMV to determine which specific type of error (interleave or fast) triggered the Flag Signal. However, if any CRC, LOS, LPR, SEF, or far-end defect were detected, the Flag Signal would not be triggered.

Use of the Flag Signal for Notification of Message Receipt

The ME can configure the ATU-C and ATU-R to set the PF4 Flag Signal when the RXDA.mailbox (Offset 11) CMV indicates that a mailbox message has been received. To use this capability, the ME must set bit 10 of FLAG.mask (Offset 0), which configures the AD20MSP918 to set the PF4 line (the Flag Signal) on receipt of a mailbox message. To clear the Flag Signal, the ME should first read the message from RXDA.data[] (Offset 1-2), then clear the mailbox flag by clearing RXDA.mailbox.

Clearing the Flag Signal

You cannot clear the Flag Signal directly. The ME may clear it by clearing the event occurrence, which initially triggered the Flag Signal; alternatively, the ME may clear it by clearing the event occurrence bit in FLAG.mask (Offset 0). For example, if receipt of a near-end mailbox message (bit 10 of FLAG.mask is set) triggers the Flag Signal, the ME can clear it in one of the following ways:

1. Clear RXDA.mailbox (Offset 11).
2. Clear bit 10 of FLAG.mask (Offset 0).

Notes

FLAG.mask (Offset 0) does NOT mask the failure indications in DIAG. It only affects the Flag Signal trigger.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Related CMVs

DIAG

Reports many of the conditions that can be used as triggers.

RXDA, TXDA

Sets the mailboxes that can be used as triggers.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

INFO (Information)

Summary

Name	O	L	Access	Description
INFO.RT_serial_number	0-7	8	ATU-C R-only ATU-R R/W	ATU-R modem Serial Number. Default at CO: 0x0 Default at RT: 0x0
INFO.RT_vendor_ID	8	1	ATU-C R-only ATU-R R/W	ATU-R ANSI EOC Vendor ID. Default at CO: 0x0 Default at RT: 0x1C
INFO.RT_version_number	9	1	ATU-C R-only ATU-R R/W	ATU-R modem Version Number. Default at CO: 0x0 Default at RT: 0x0
INFO.RT_fw_version	10	1	ATU-R R-only ATU-C R-only	Firmware version on the ATU-R modem. An ATU knows the firmware version of the other ATU, if G.hs was used.
INFO.CO_fw_version	11	1	ATU-C R-only ATU-R R-only	Firmware version on the ATU-C modem. An ATU knows the firmware version of the other ATU, if G.hs was used.
INFO.candidate_number	12	1	ATU-C R-only ATU-R R-only	Candidate number of the firmware version resident on the modem.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access	Description
INFO.ANSI_rt_ID	13	1	ATU-C R-only ATU-R R-only	Returns the ANSI Link Initiation Vendor ID of the ATU-R.
INFO.ANSI_co_ID	14	1	ATU-C R-only ATU-R R-only	Returns the ANSI Link Initiation Vendor ID of the ATU-C.
INFO.Chips_ver	15	1	ATU-C R-only ATU-R R-only	Returns the Version Number of 6438/6449 and flash/SRAM.
INFO.itu_rt_ID	17 18	2	ATU-C R-only ATU-R R-only	ITU Vendor ID (8bytes) of ATU-R
INFO.itu_co_ID	19 20	2	ATU-C R-only ATU-R R-only	ITU Vendor ID (8bytes) of ATU-C
INFO.itu_rt_eoc_ID	21 22	2	ATU-C R-only ATU-R R/W	ITU Vendor ID to be exchanged over EOC for G.hs links.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

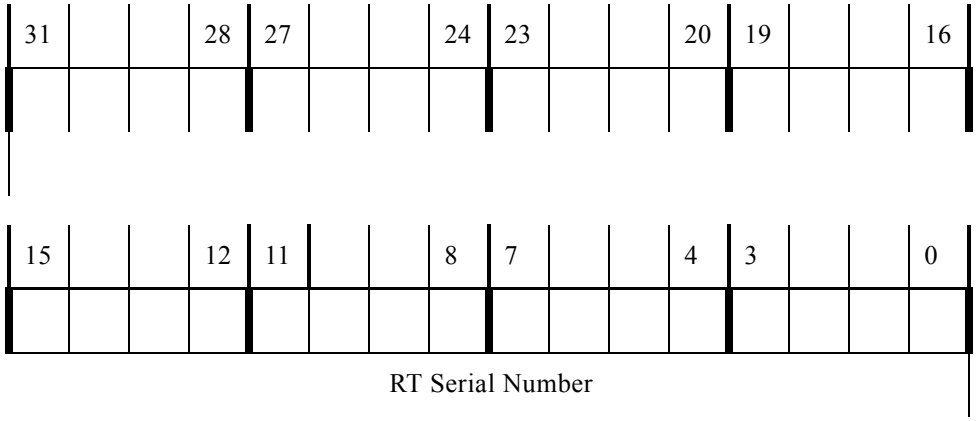

Figure 39. INFO.RT_serial_number (offset 0-7)

All 256 bits of INFO offset 0-7 are used to transport the RT Serial Number.

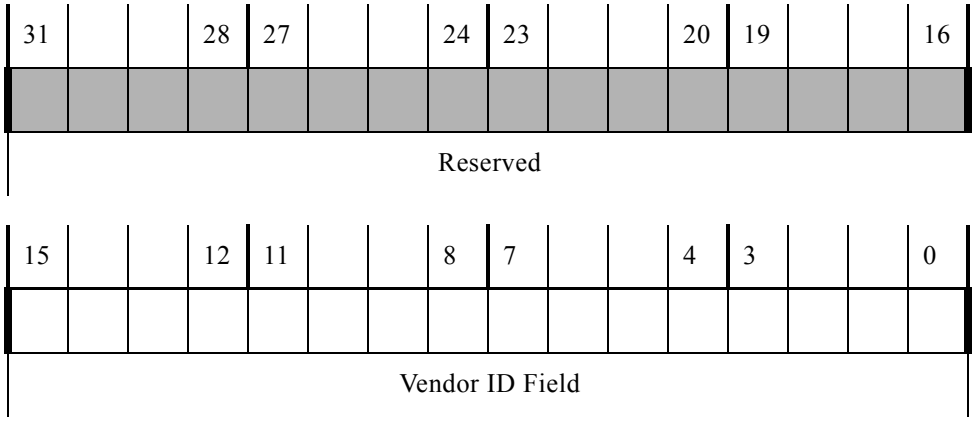

Figure 40. INFO.RT_vendor_ID (offset 8)

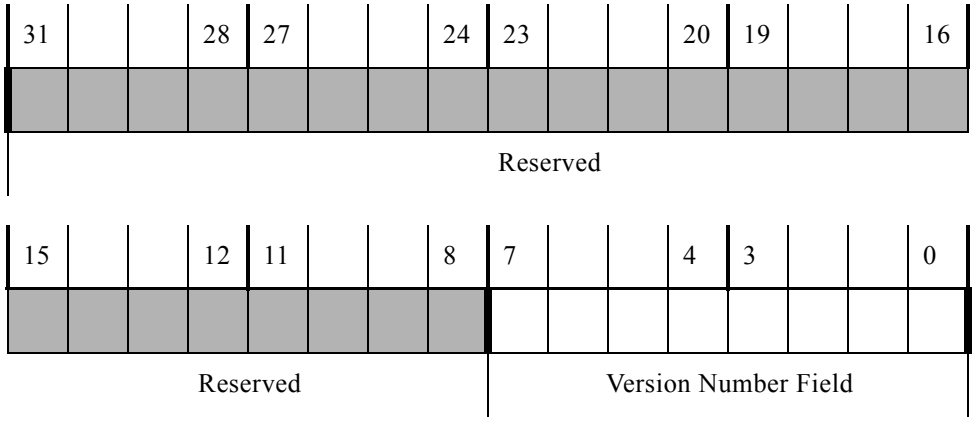

Figure 41. INFO.RT_version_number (offset 9)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Figure 42. INFO.RT_fw_version (INFO offset 10) and INFO.CO_fw_version (INFO offset 11)

31			28	27			24	23			20	19			16

Firmware Version

15			12	11			8	7			4	3			0

Firmware Version

INFO.RT_fw_version (INFO offset 10) and INFO.CO_fw_version (INFO offset 11) use all 31 bits each to store the firmware version number.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

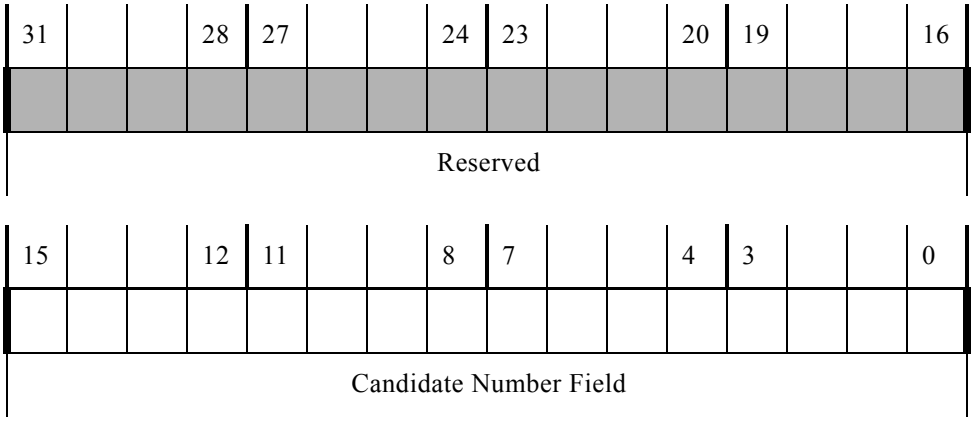

Figure 43. INFO.candidate_number (offset 12)

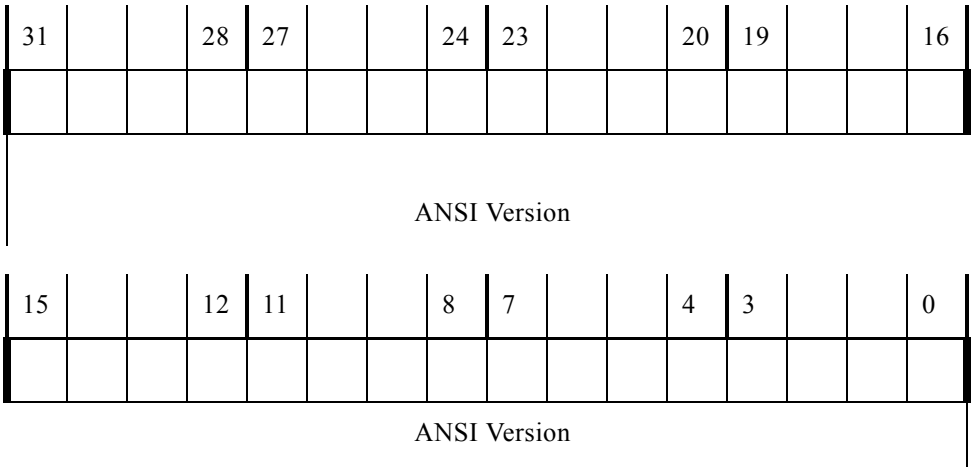

Figure 44. INFO.ANSI_rt_ID (INFO offset 13) and INFO.ANSI_co_ID (offset 14)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Flash/SRAM type															

15			12	11			8	7			4	3			0
6438/6449 version															

Figure 45. INFO.CHIPS_ver (offset 15)

31			28	27			24	23			20	19			16
Country Code															

15			12	11			8	7			4	3			0
(upper 2 bytes of) Provider Code															

Figure 46. INFO.ITU_rt_ID (INFO offset 17), INFO.ITU_co_ID (INFO offset 19), and INFO.ITU_rt_eoc_ID (INFO offset 21).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

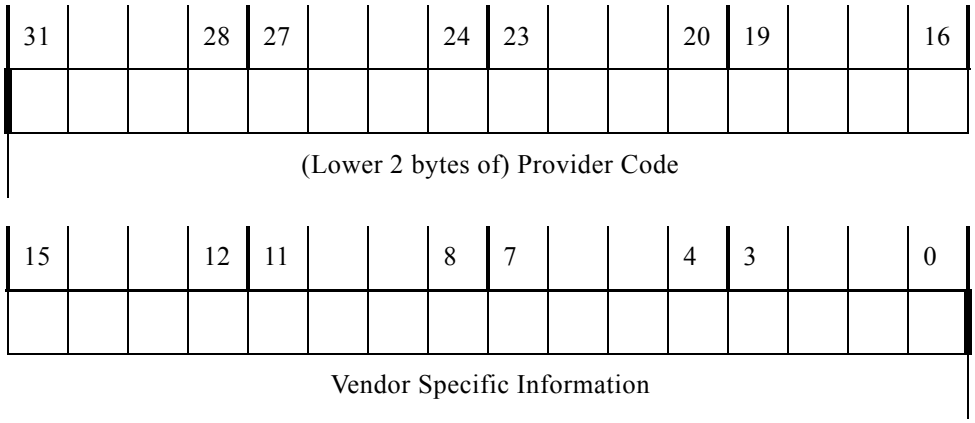

Figure 47. INFO.ITU_rt_ID (INFO offset 18), INFO.ITU_co_ID (INFO offset 20), and INFO.itu_rt_eoc_ID (INFO offset 22),

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 34 INFO.ITU_rt_ID (INFO offset 17), INFO.ITU_co_ID (INFO offset 19), and INFO.ITU_rt_eoc_ID (INFO offset 21).

Bit	Name	**Description**
15:0	Upper 2 bytes of Provider Code	Upper2bytesofITUProviderCode. Default: 0X414E **NOTE**: The lower 2 bytes of the ITU Provider Code are in the INFO offset 18, 20, and 22.
31:16	Country Code	ITU Country Code Default: 0X0

Table 35 INFO.ITU_rt_ID (INFO offset 18), INFO.ITU_co_ID (INFO offset 20), and INFO.ITU_rt_eoc_ID (INFO offset 22)

Bit	Name	**Description**
15:0	Vender Specific Information	Default: 0x0
31:16	Lower 2 bytes of Provider Code	Lower 2 bytes of ITU Provider Code. Default: 0X4456 **NOTE**: The upper 2 bytes of the ITU Provider Code are in the INFO offset 17,19, and 21.

At the CO, INFO.ITU_rt_ID (INFO offset 17, 18) default to 0 on reboot. If the link trains in G.hs, then the CO will populate INFO.ITU_rt_ID with information it receives from the RT. If the link trains in T1.413 mode then INFO.ITU_rt_ID will remain 0 at the CO.

At the RT, INFO.ITU_co_ID (INFO offset 19, 20) default to 0 on reboot. If the link trains in G.hs, then the RT will populate INFO.ITU_co_ID with information it receives from the CO. If the link trains in T1.413 mode the INFO. ITU_co_ID will remain 0 at the RT.

At the CO, INFO.ITU_rt_eoc_ID (INFO offset 21, 22) default to 0 on reboot. If the link trains using G.hs and firmware is Release 3.1 or later and EOC ID read command has been completed, then the CO will populate INFO.ITU_rt_eoc_ID with information it receives from the RT over the EOC channel. Otherwise INFO.ITU_rt_eoc_ID remains 0 at the CO.

NOTE: For links that train in T1.413 mode, INFO offset 8 is used for RT EOC Vendor ID.

Usage

The INFO CMV provides configuration information about the ADI Chipset and associated firmware. Some INFO require the ATU-C to be capable of reading the Serial Number, Vendor ID, and Version Number of the ATU-R through the EOC channel.

The ME-R must use INFO to load these three pieces of information to the ATU-R prior to link initiation. The ATU-R passes them to the ATU-C, where they are available to the ME-C upon request.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

If the ME-R supplies no configuration information, the INFO.RT_vendor_ID (INFO offset 8) will default to a Vendor ID of 0x001C for the ATU-R. The default for the remaining INFOs are zeros.

Notes

The candidate number of INFO.candidate_number (INFO offset 12) is for ADI internal use only.

Related CMVs

None.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

INTL (Interleave)

Table 36 INTL.downstream (offset 0)

Name	O	L	Access	Description
INTL.downstream	0	1	ATU-C R-only ATU-R R-only	Reports the current interleave depth, symbols per codeword and latency Downstream.

Bit	Name	Description
7:0	interleave depth	Reports interleave depth in bytes
15:8	Reserved	
23:16	Sym/CW DS	Reports symbols per codeword Downstream
31:24	DS Latency	Reports Downstream latency in .25 ms steps

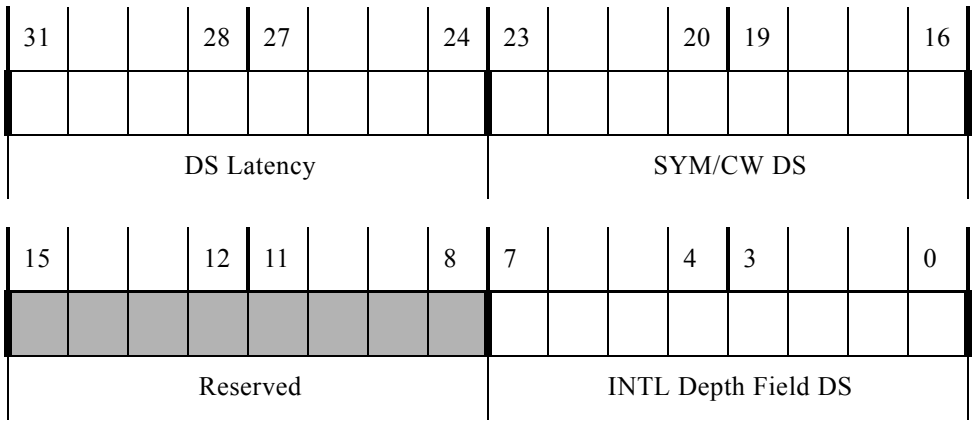

Figure 48. INTL.downstream (offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 37 INTL.upstream (offset 1)

Name	O	L	Access	Description
INTL.upstream	1	1	ATU-C R-only ATU-R R-only	Reports the current interleave depth, symbols per codeword and latency Upstream.

Bit	Name	Description
7:0	interleave depth	Reports interleave depth in bytes
15:8	Reserved	
23:16	Sym/CW US	Reports symbols per codeword Upstream
31:24	US Latency	Reports Upstream latency in .25 ms steps

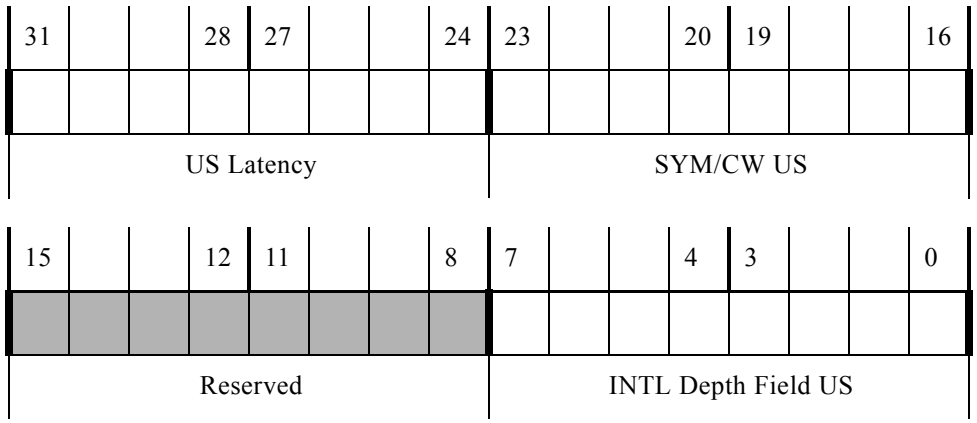

Figure 49. INTL.upstream (offset 1)

Usage

INTL reports the Interleave depth in bytes.

Notes

None.

Related CMVs

ADPT.downstream (ADPT offset 0)

ADPT.upstream (ADPT offset 1)

These variables set the Interleave depth for Old Interface Rate Adaptive links.

ADPT.ds_latency (ADPT offset 5)

ADPT.us_latency (ADPT offset 7)

These variables set the Max Interleave depth for New Interface Rate Adaptive links.

DOPT.intl_depth (DOPT offset 5)

UOPT.intl_latency (UOPT offset 5)

These variables set the Interleave depth for Explicit Rates links.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

MASK

Summary

Name	O	L	Access	Description
MASK.downstream	0-7	8	ATU-C R/W	Enables or disables a specified set of tones in the DS datapath.
MASK.upstream	8	1	ATU-C R/W ATU-R R/W	Enables or disables a specified set of tones in the US datapath. Default: 0x1FFFFFC0 (POTS) 0xF0000000 (ISDN)
MASK.downstream	9	1	ATU-C R/W ATU-R R/W	Enables or disables a specified set of tones in the US datapath. Default: 0xFFFFFFFF (ISDN only)

Figure 19-2 through Figure 19-16 summarize the mapping and restrictions on the use of these mask bits. The MASK layout varies between Full-rate Mode and Lite Mode.

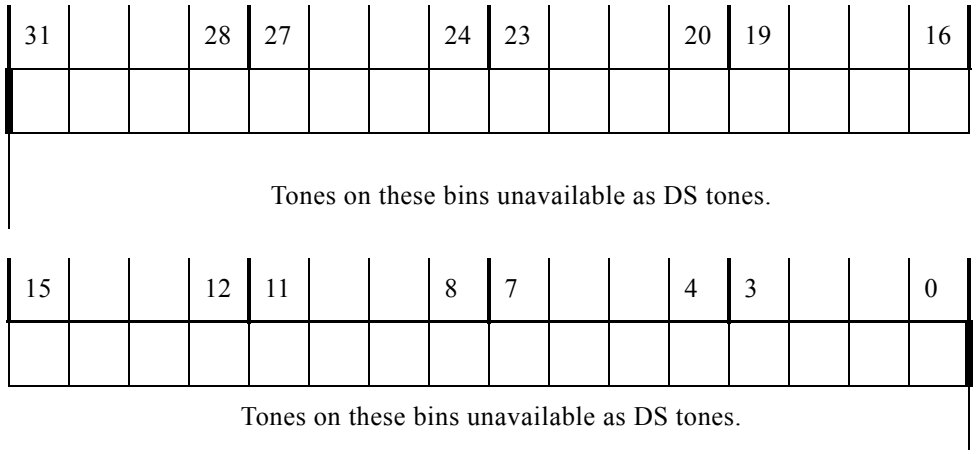

Figure 50. MASK.downstream, (MASK offset 0), Full rate (POTS\ISDN)

31			28	27			24	23			20	19			16
Bin 63	Bin 62	Bin 61	Bin 60	Bin 59	Bin 58	Bin 57	Bin 56	Bin 55	Bin 54	Bin 53	Bin 52	Bin 51	Bin 50	Bin 49	Bin 48
15			12	11			8	7			4	3			0
Bin 47	Bin 46	Bin 45	Bin 44	Bin 43	Bin 42	Bin 41	Bin 40	Bin 39	Bin 38	Bin 37	Bin 36	Bin 35	Bin 34	Bin 33	Bin 32

Figure 51. MASK.downstream, (MASK offset 1), (POTS)

31			28	27			24	23			20	19			16
Bin 63	Bin 62	Bin 61	Bin 60	Bin 59	Bin 58	Bin 57	Bin 56	Bin 55	Bin 54	Bin 53	Bin 52	Bin 51	Bin 50	Bin 49	Bin 48
15			12	11			8	7			4	3			0
Bin 47	Bin 46	Bin 45	Bin 44	Bin 43	Bin 42	Bin 41	Bin 40	Bin 39	Bin 38	Bin 37	Bin 36	Bin 35	Bin 34	Bin 33	Bin 32

Figure 52. MASK.downstream, (MASK offset 9)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Bin 95	Bin 94	Bin 93	Bin 92	Bin 91	Bin 90	Bin 89	Bin 88	Bin 87	Bin 86	Bin 85	Bin 84	Bin 83	Bin 82	Bin 81	Bin 80
15			12	11			8	7			4	3			0
Bin 79	Bin 78	Bin 77	Bin 76	Bin 75	Bin 74	Bin 73	Bin 72	Bin 71	Bin 70	Bin 69	Bin 68	Bin 67	Bin 66	Bin 65	Pilot Tone (POTS)

Figure 53. MASK.downstream, (MASK offset 2), (Full-rate POTS/ISDN)

31			28	27			24	23			20	19			16
Bin 127	Bin 126	Bin 125	Bin 124	Bin 123	Bin 122	Bin 121	Bin 120	Bin 119	Bin 118	Bin 117	Bin 116	Bin 115	Bin 114	Bin 113	Bin 112
15			12	11			8	7			4	3			0
Bin 111	Bin 110	Bin 109	Bin 108	Bin 107	Bin 106	Bin 105	Bin 104	Bin 103	Bin 102	Bin 101	Bin 100	Bin 99	Bin 98	Bin 97	Pilot Tone (ISDN)

Figure 54. MASK.downstream, (MASK offset 3)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Bin 159	Bin 158	Bin 157	Bin 156	Bin 155	Bin 154	Bin 153	Bin 152	Bin 151	Bin 150	Bin 149	Bin 148	Bin 147	Bin 146	Bin 145	Bin 144

15			12	11			8	7			4	3			0
Bin 143	Bin 142	Bin 141	Bin 140	Bin 139	Bin 138	Bin 137	Bin 136	Bin 135	Bin 134	Bin 133	Bin 132	Bin 131	Bin 130	Bin 129	Bib 128

Figure 55. MASK.downstream, (MASK offset 4)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Bin 191	Bin 190	Bin 189	Bin 188	Bin 187	Bin 186	Bin 185	Bin 184	Bin 183	Bin 182	Bin 181	Bin 180	Bin 179	Bin 178	Bin 177	Bin 176
15			12	11			8	7			4	3			0
Bin 175	Bin 174	Bin 173	Bin 172	Bin 171	Bin 170	Bin 169	Bin 168	Bin 167	Bin 166	Bin 165	Bin 164	Bin 163	Bin 162	Bin 161	Bib 160

Figure 56. MASK.downstream, (MAST offset 5), Full-rate (POTS /ISDN)

31			28	27			24	23			20	19			16
Bin 223	Bin 222	Bin 221	Bin 220	Bin 219	Bin 218	Bin 217	Bin 216	Bin 215	Bin 214	Bin 213	Bin 212	Bin 211	Bin 210	Bin 209	Bin 208
15			12	11			8	7			4	3			0
Bin 207	Bin 206	Bin 205	Bin 204	Bin 203	Bin 202	Bin 201	Bin 200	Bin 199	Bin 198	Bin 197	Bin 196	Bin 195	Bin 192	Bin 193	Bib 192

Figure 57. MASK.downstream, (MASK offset 6), Full rate.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Bin 255	Bin 254	Bin 253	Bin 252	Bin 251	Bin 250	Bin 249	Bin 248	Bin 247	Bin 246	Bin 245	Bin 244	Bin 243	Bin 242	Bin 241	Bin 240
15			12	11			8	7			4	3			0
Bin 239	Bin 238	Bin 236	Bin 236	Bin 235	Bin 234	Bin 233	Bin 232	Bin 231	Bin 230	Bin 229	Bin 228	Bin 227	Bin 226	Bin 225	Bib 224

Figure 58. MASK.downstream, (MASK offset 7), Full rate.

31			28	27			24	23			20	19			16
	Bin 30	Bin 29	Bin 28	Bin 27	Bin 26	Bin 25	Bin 24	Bin 23	Bin 22	Bin 21	Bin 20	Bin 19	Bin 18	Bin 17	Bin 16
15			12	11			8	7			4	3			0
Bin 15	Bin 14	Bin 13	Bin 12	Bin 11	Bin 10	Bin 9	Bin 8	Bin 7	Bin 6	Unavailable bins					

Figure 59. MASK.upstream (MASK offset 8), Full rate and Lite.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

MASK writes a set of tone enablements and disablements for US and DS. A disabled tone can be asserted, but the ATU does not respond to it for certain purposes explained below.

MASK.downstream contains 256 bits in 7 datawords and MASK.upstream contains 32 bits in one dataword. Each bit enables or disables one tone. You may have noted that the number of bits does not match the number of tones. That is because not every bit accesses a valid tone.

For MASK.upstream (Offset 8), the lsb corresponds to the tone on bin 0 and the msb corresponds to the tone on bin 31. Similarly, the lsb of MASK.downstream, Offset 0, also corresponds to the tone on bin 0, but you are not allowed to use it, as it is upstream. The msb of MASK.downstream, Offset 7, corresponds to the tone for bin 255 (which is downstream).

Design constraints made a more direct mapping scheme unavailable. The limitations are given in Table 20. Note that they follow nearly the same restrictions as for the TONE CMV:

Table 38 MASK Restrictions

Tones	Upstream	Downstream
Total number of bins and tones.	31	255
Default, Full-rate	Tones on bins 6-28	Tones on bins 31-254
Default, Lite	Tones on bins 6-28	Tones on bins 33-127
Unavailable even if enabled by MASK	Tones on bins 0-5, 31	Tones on bins 0-30 (actually upstream) bin 255
Available if enabled through MASK	Tones on bins 29-30. Must be enabled at both ATU-C and ATU-R.	None

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

These uses apply:

- When MASK.downstream disables tones at the ATU-C and MASK.upstream disables them at the ATU-R, modem training does not use the disabled tones.
- When MASK.upstream disables tones at the ATU-C, the training may use the disabled tones, but the DMT logic allocates no bits to those tones.
- MASK.downstream is not available at the ATU-R.

Notes

1. MASK cannot disable the pilot tone, which is on bin 64.
2. The modem also applies tone masking to the wide-band test signal generated by TEST.control (TEST offset 0).

Related CMVs

TONE

Reads the transfer characteristics of a tone on one bin.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

OPTN (Options)

Summary

Name	O	L	Access	Description
OPTN.options	0	1	ATU-C R/W ATU-R R/W	Indicates availability and/or use of specific features. Default: 0x00000044
OPTN.bitswap	1	1	ATU-C R/W ATU-R R/W	Configurations for the bitswap feature. Default is 0x00000994.
OPTN.utopia	2	1	ATU-C R/W ATU-R R/W	Configures the ATM/UTOPIA interface. Default: 0x01500000
OPTN.fdq	3	1	ATU-C R/W ATU-R R/W	Enables or disables FDQ.
OPTN.adsl_standard	4	1	ATU-C R/W ATU-R R/W	User-programmed register to select ADSL standard options.
OPTN.cpr_01	5	1	ATU-C R/W ATU-R R/W	User-programmed register used for CPR software work-arounds and miscellaneous configurations.
OPTN.930	6	1	ATU-C R/W ATU-R R/W	Configuration for AD20MSP930 Chipset. Selects “Normal” or “Standby” mode.
OPTN.atm_fifo	7*	1	ATU-C R/W ATU-R R/W	Configures the ATM FIFOs of the AD6438/6449. (Bits 15:0 are reserved for Anaconda/Eagle applications)

***Anaconda/Diamondback/Eagle Specific CMV**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Name	O	L	Access	Description
OPTN.atm_fifo_new	13*	1	ATU-C ATU-R	Sets up general Loopback features such as ATM addresses, Utopia level, Tx mode, ADSL and ATM scrambling
OPTN.atm_fifo_new	14*	1	ATU-C ATU-R	Sets up the Tx and intl latency path rates in Loopback mode
OPTN.atm_fifo_new	15*	1	ATU-C ATU-R	This sets up the Tx and Rx FIFO sizes in each latency path

***Anaconda/Diamondback/Eagle Specific CMV**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 39 OPTN.options (OPTN offset 0)

Bit	Name	Description
0	EC Available	0 Echo Canceller (EC) not available. 1 Available.
1	TCM Available	0 Trellis coded Modulation (TCM) not available. 1 Available.
2	FDQ Adaption Available	0 FDQ Adaption not available. 1 Available.
4	EC Config	0 Use EC if available. 1 Do not use.
5	TCM Config	0 Do not use TCM. 1 Use TCM if available.
6	FDQ Adaption Config	0 Do not use FDQ Adaption on margin loss. 1 Use FDQ Adaption on margin loss.
8	EC In Use	0 EC not in use. 1 In use.
9	TCM In Use	0 TCM not in use. 1 In use.
10	FDQ Adaption In Use	0 FDQ Adaption not currently in use. 1 In use.
11	RA Fast Path Margin Setting	0 Set Fast-path Margin to 6dB (Rate-adaptive Configuration only). 1 Set Fast-path Margin to value in ADPT (Rate-adaptive Configuration only).
12	Reserved	0 Reserved 1 Reserved
16:14	PGA Cutback Offset	The value, 0-7 dB, to be subtracted from the nominal PGA cutback.
17	Cutback Power (ATU-R only)	0 Normal operation (default). 1 Use cutback power at the ATU-R for loops with a high echo. This improves performance in loops with bridge taps.
18	Local NTR	0 Disable NTR at the local ATU. 1 Enable NTR at the local ATU.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 39 OPTN.options (OPTN offset 0)

Bit	Name	Description
19	Remote NTR	0 Disable NTR at the remote ATU. 1 Enable NTR at the remote ATU.
20	Clear Profiles	0 Default. Do not clear profile settings for fast retrain. 1 Clear profiles. NOTES: 1. The ME-C or ME-R must set the bit prior to a full initialization. 2. If an ATU receives a CMV with this bit set, it will not clear profiles until it performs a full initialization. 3. The bit is reset to zero after profiles have been cleared.
21	Manual Fast Retrain	0 Do not perform a manually triggered fast retrain (default). 1 Perform a manual fast retrain.
22	Reboot to Train Enable	0 Enable autoreboot to full-train if no profile match is found (default). 1 Disable autoreboot. The ATU will instead transition to FAIL if it makes no profile match.
23	Autoinitiate Fast Retrain Enable	0 Disable autoinitiation of a fast retrain (ATU-C default). 1 Enable (ATU-R default). NOTE: This bit will be automatically cleared if the ATU links in Full-rate Mode.
24	Profile FLASH/RAM Access Control	0 Use FLASH access for profiles (default). This enables FLASH unlock. 1 Use RAM access for profiles. This disables FLASH unlock.
25	Fast Retrain Enable/Disable	0 Default. Enable Fast Retrain. 1 Disable all Fast Retrain at the highest level.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 39 OPTN.options (OPTN offset 0)

Bit	Name	Description
27	RA Mode Rate Limit US (ATU_C ONLY)	0 The US data rate will be limited to the smaller of the Max Data Rate from the ADPT settings or 864 kbps (918) or 960 (930) (Default) 1 The USdata rate will be is limited only by the ADPT settings
28	RA Mode Neg Margin DS	0 The margin requirement in ADPT.downstream is a positive number. 1 The margin requirement in ADPT.downstream is a negative number.
29	RA Mode Neg Margin US	0 The margin requirement in ADPT.upstream is a positive number. 1 The margin requirement in ADPT.upstream is a negative number.
31	Alternate PF7 Op	0 PF 7 will toggle when the modem is OPERATIONAL. At all other times, PF7 will be low. 1 PF7 will toggle while the modem is initializing a link. PF7 will be high when the modem is OPERATIONAL. At all other times, PF7 will be low.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Alternate PF7 Op	Reserved	RA Mode Neg Margin US	RA Mode Neg Margin US	RA Mode US rate limited (ATU_C only)	Reserved	FR Enable	Profile Flash/RAM Access control	Auto initiate FR enable	Reboot to train enable	Manual Fast Retain	Clear Profiles	Remote NTR	Local NTR	Cutback Power	

15			12	11			8	7			4	3			0
PGA Cutback Offset		Reserved	RA Margin Mode	RA Fast Path Margin Setting	FDQ Adaption In Use	TCM In Use	EC In Use	Reserved	FDQ Adaption Config	TCM Config	EC Config	Reserved	FDQ Adaption Available	TCM Available	EC Available

Figure 60. OPTN.options (offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 40 OPTN.bitswap (OPTN offset 1)

Bits	Name	Description
3:0	Bitswap Mode	0000 Bitswap Mode 0. Bitswap off. 0001 Bitswap Mode 1. Full bitswap on, including initiating and accepting bitswap request messages. 0010 Bitswap Mode 2. Bitswap on, but only for accepting bitswap request messages. 0100 Bitswap Mode 4. Always reply UTC (Unable To Comply) on receipt of a bitswap request message (default).
7:4	Move From Delta	The threshold difference, in dB, between the SNR value of a “bad” bin and the desired margin, required for removal of the bit.
11:8	Move To Delta	The threshold difference, in dB, between the SNR value of a “good” bin and the desired margin, required for acquiring the bit.
12	Self-test	0 Has no effect. 1 Manual bitswap: sends out a bitswap request if the Bitswap Mode value is 0001 and there is a reset on successful start of a self-test.
23:16	From Bin Number	Reset on successful start of a self-test in a manual bitswap. The number of the bin from which the bit is to be moved.
31:24	To Bin Number	Reset on successful start of a self-test in a manual bitswap. The number of the bin to which the bit is to be moved.

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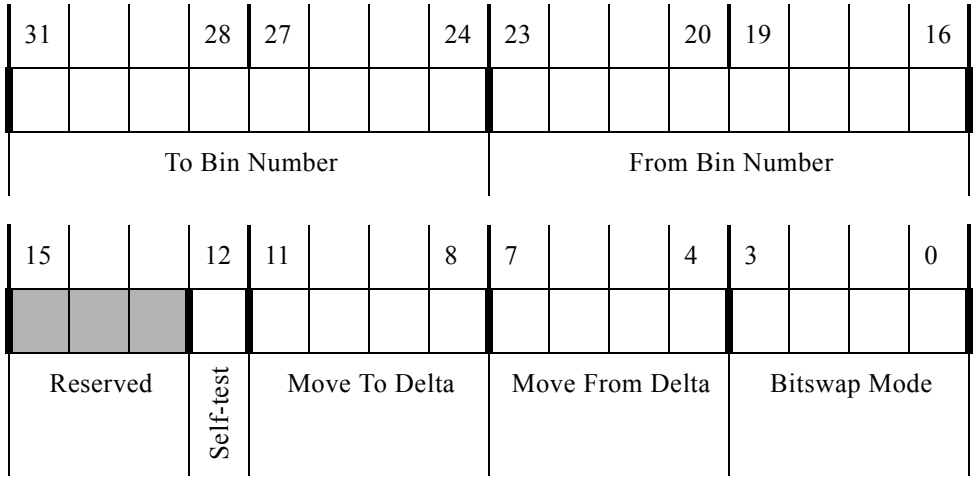


Figure 61. OPTN.bitswap (offset 1)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 41 OPTN.utopia (offset 2)

Bits	Name	Description
4:0	Tx Fast Path Address	ATM address for the Tx port on Fast Path. • The range for the values of this and the next three fields is 0x00 through 0x1E. • 0x1F is reserved.
9:5	Rx Fast Path Address	ATM address for the Rx port on Fast Path.
14:10	Tx Intl Path Address	ATM address for the Tx port on Interleave Path.
19:15	Rx Intl Path Address	ATM address for the Rx port on Interleave Path.
20*	Reserved	0 Default NOTE: (Anaconda/Eagle operation) Bit 20 of OPTN.utopia is no longer assigned to 'CLAV Config'. It is reserved bit for Anaconda/Diamondback and Eagle applications.
21	CLAV Mode	0 Select MCLAV, Multiple CLAV Mode (default). 1 Select SCLAV, Single CLAV Mode.
22	PHY Mode	0 Select MPHY, Multiple PHY Mode. Configures the AD20MSP918 to interface with multiple physical layers. 1 Select SPHY, Single PHY Mode. Configures the AD20MSP918 to interface with a single physical layer. This is the default.
23	ATM/STM	0 Select Asynchronous Transfer Mode (ATM), which is the default. 1 Select Serial Transfer Mode (STM).
25:24	Framing Mode	Selects the desired framing mode. 00 Framing Mode 0, serial mode. 01 Framing Mode 1, full overhead (default). 10 Framing Mode 2, reduced overhead, separate fast and sync bytes. 11 Framing Mode 3, reduced overhead, merged fast and sync bytes.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 41 OPTN.utopia (offset 2)

Bits	Name	Description
26	Cell/Octet Mode	0 Select Cell Mode (default). Flow control is at the cell level. 1 Select Octet mode. Flow control is at the octet level.
27	ATM Scrambling	0 Turn ATM scrambling on. (default) 1 Turn it off. **NOTE:** **You should only disable scrambling for debugging purposes.**
28	ADSL Scrambling	0 Turn ATM scrambling on. (default) 1 Turn it off. **NOTE:** **You should only disable scrambling for debugging purposes.**
29	DS Multiframe Code-words (MFC)	0 Use only 1 DS frame per codeword in Rate-adaptive Configuration when the coding is on (default). 1 Use multiple frames (improves FEC efficiency).
30*	Reserved	0 Default. Note: (Anaconda/Eagle operation) Bit 30 of OPTN.utopia is no longer assigned to 'Drop HEC Enable'. It is a reserved bit for Anaconda/Diamondback and Eagle applications.

*** These bits are reserved for Anaconda/Eagle operation**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

31			28	27			24	23			20	19			16
Re served	*Reserved	DS MFC	ADSL Scrambling	ATM Scrambling	Cell/Octet Mode	Fram-ing Mode		ATM/STM	PHY Mode	CLAV Mode	*Reserved	19:15 Rx Intl Path Address			

15			12	11			8	7			4	3			0
	Tx Intl Path Address					Rx Fast Path Address					Tx Fast Path Address				

*** These bits are reserved for Anaconda/Eagle operation**

Figure 62. OPTN.utopia (offset 2)

Table 42 OPTN.fdq (offset 3)

Bits	Name	Description
0	Reserved	
1	CRC FDQ	0 Don't do FDQ on detection of CRC burst. 1 Do FDQ, etc. (Default)
2	FEC FDQ	0 Don't do FDQ on detection of FEC. 1 Do FDQ, etc. (Default)
3	Always FDQ	0 FDQ not always on.(Default) 1 Always on.
4	Never FDQ	0 FDQ not always off. (Default) 1 Always off (overrides bit 3).
5	Bias FDQ	0 Clear FDQ bias. 1 Set FDQ bias.(Default)
31:16	FDQ Adaption Count	The number of FDQ adaptions since entering present SHOWTIME.

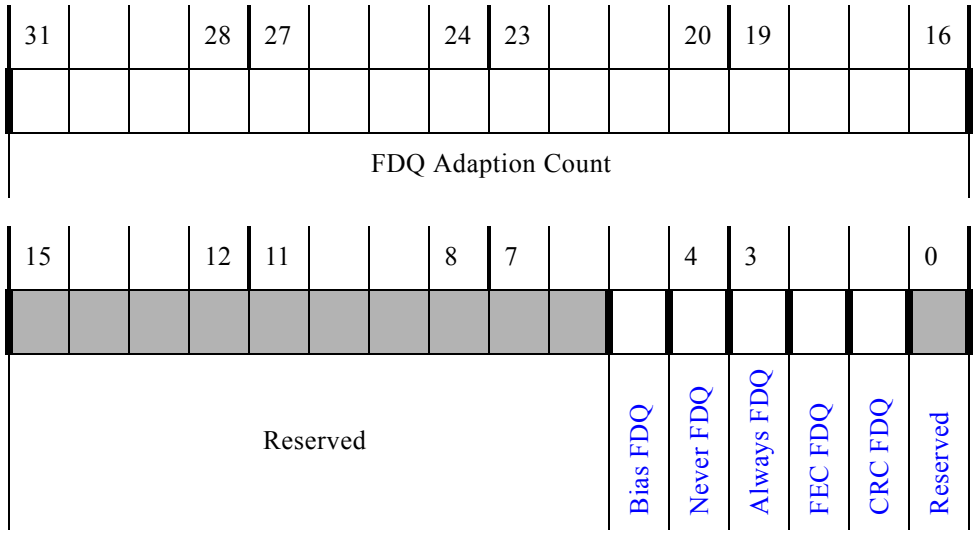


Figure 63. OPTN.fdq (offset 3)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 43 ATU-C OPTN.adsl_standard (offset 4)

Bits	Name	Description
1:0	Std_Select	ADSL Standard in effect. 00 G.992.x/G994.1 is preferred, but T1.413 is allowed. 01 Use G.992.x/G.994.1 only. 10 Default. Use T1.413 only. 11 T1.413 is preferred, but G.992.x/G.994.1 is allowed.
5:4	G992.x_Select	00 Default. Use either G992.1 Annex A (Full-rate Mode) or G992.2 Annex A/B (Lite Mode). 01 Use only G992.1 Annex A (Full-rate Mode). 10 Use only G992.2 Annex A/B (Lite Mode).
9	Immediate_FR	0 Default. G992.2 Fast Retrain after initial handshake is disabled. 1 G992.2 Fast Retrain after initial handshake is enabled. This bit is cleared after the FR is run.
10	MS_Response	G994.1 Mode Select (MS) Response. 0 Default. Transmits ACK 1 if Capability Lists have been exchanged; otherwise, transmits a REQ-CLR (Request Capability List Request). 1 Transmits REQ-MR (Request Mode Request) if Capability Lists have been exchanged; otherwise, transmits a REQ-CLR (Request Capability List Request).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 43 ATU-C OPTN.adsl_standard (offset 4)

Bits	Name	Description
11	MR_Response	G994.1 Mode Request (MR) Response. 0 Default. Transmits an MS (Mode Select) if Capability Lists have been exchanged; otherwise, transmits a REQ-CLR (Request Capability List Request). 1 Transmits a REQ-MS (Request Mode Select) if Capability Lists have been exchanged; otherwise, transmits a REQ-CLR.

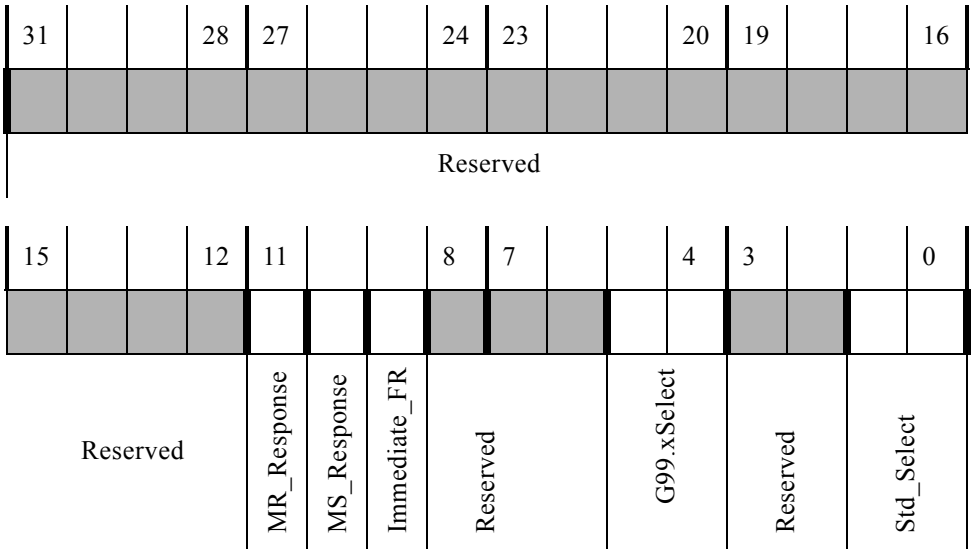


Figure 64. ATU-C OPTN.adsl_standard (offset 4)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 44 ATU-R OPTN.adsl_standard (offset 4)

Bits	Name	Description
1:0	Std_Select	ADSL Standard in effect. 00 G.992.x/G994.1 is preferred, but T1.413 is allowed. 01 Use G.992.x/G.994.1 only. 10 Use T1.413 only. (Default) 11 Reserved.
5:4	G992.x_Select	00 Use either G992.1 Annex A/B (Full-rate Mode) or G992.2 Annex A (Lite Mode). (Default) 01 Use only G992.1 Annex A/B (Full-rate Mode). 10 Use only G992.2 Annex A (Lite Mode).
9	Immediate_FR	0 G992.2 Fast Retrain after initial handshake is disabled. (Default) 1 G992.2 Fast Retrain after initial handshake is enabled. This bit is cleared after the FR is run.
10	Init_TX_msg	Initial Transmit Message. 0 Default. Transmits MS (Mode Select) if Capability Lists have been exchanged; otherwise, transmits a CLR (Capability List Request). 1 Transmits MR (Mode Request) if Capability Lists have been exchanged; otherwise, transmits a CLR (Capability List Request).
11	Reserved	Is reserved on the RT.
12	Reserved	
13	FR_Abort	ATU-R only 0 - RT will not initiate FR abort. (Default) 1- RT will initiate FR abort upon entering FR after G.hs (once). The ATUs will re-enter G.hs and then perform the usual immediate _ FR.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 44 ATU-R OPTN.adsl_standard (offset 4)

Bits	Name	Description
14	Reserved	
15	Enable EOC	0 - Disable EOC operation 1- Enable EOC operation (Refer to application note ANCMV-04)

Figure 65. ATU-R OPTN.adsl_standard (offset 4)

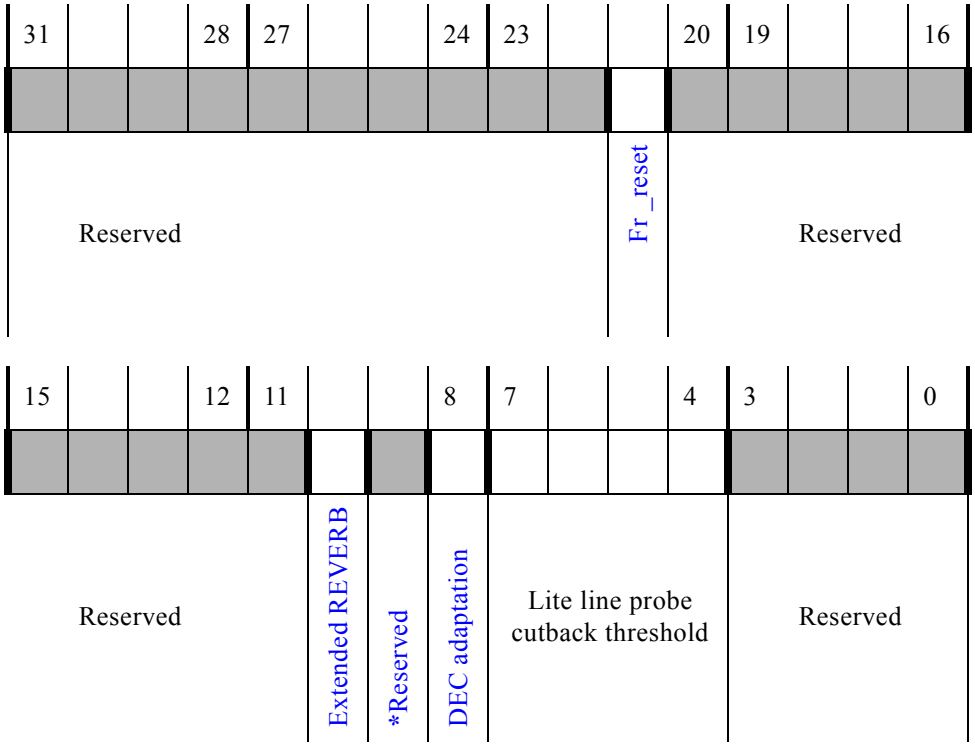
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 45 OPTN.cpr_01 (offset 5)

Bits	Name	Description
4-7	Lite line probe cut-back threshold	Left-shift the line-probe cutback threshold. A higher number means less cutback. Setting all four bits disables cutback entirely.
8	DEC adaption (ATU-C only)	0 Do not use DEC adaptation during show-time. (Default) 1 Use DEC adaptation in showtime.
9*	Reserved	0 (Default) Note: Bit 9 of OPTN.cpr_01 is no longer assigned to 'cpr_60'. It is a reserved bit for Anaconda/Diamondback/Eagle operation.
10	Extended REVERB (ATU-R only)	0 Use narrow REVERB (Default) 1 Extend REVERB and SEGUE training sig-nal (RT-only).
21	FR Reset	0 No FR Rest initiation (Default) 1 The ATU upon a unsuccessful FR, will attempt two more FR's before going back to initialization/full train states.

***This bit is reserved for Anaconda/Diamondback/Eagle Operation**

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.



***This bit is reserved for Anaconda/Diamondback/Eagle Operation**

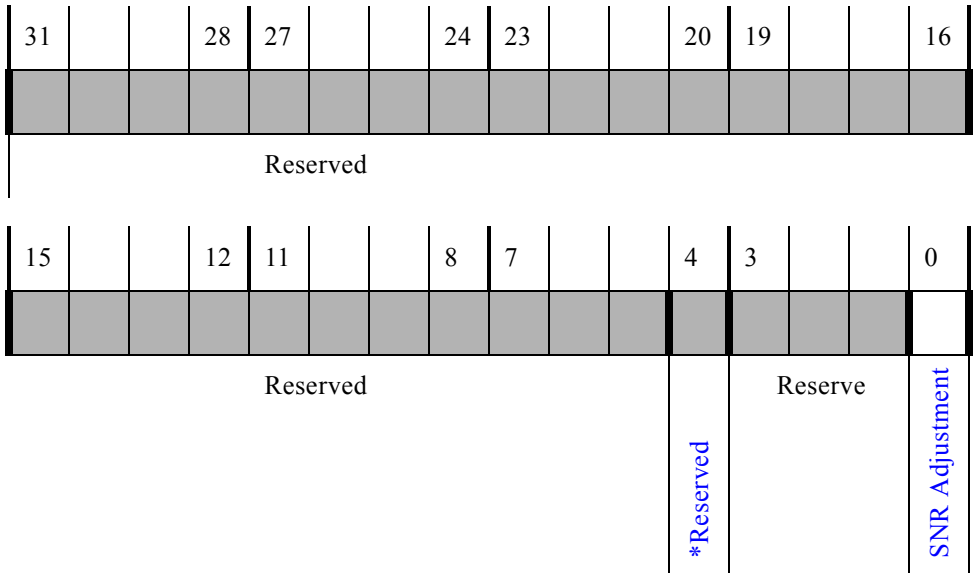
Figure 66. OPTN.cpr_01 (offset 5)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 46 OPTN.930 (offset 6)

Bits	Name	Description
0	SNR Adjustment	1 Enable SNR Adjustment based on the difference between SNRdB_Table 1 and SNRdB_Table 3. 0 Disable SNR Adjustment
3:1	Reserved	
4*	Reserved	0 (Default) Note: Bit 4 of OPTN.930 is no longer assigned to 'Normal Standby'. It is a reserved bit for Anaconda/Diamondback/Eagle operation
31:5	Reserved	

***This bit is reserved for Anaconda/Diamondback/Eagle Operation**



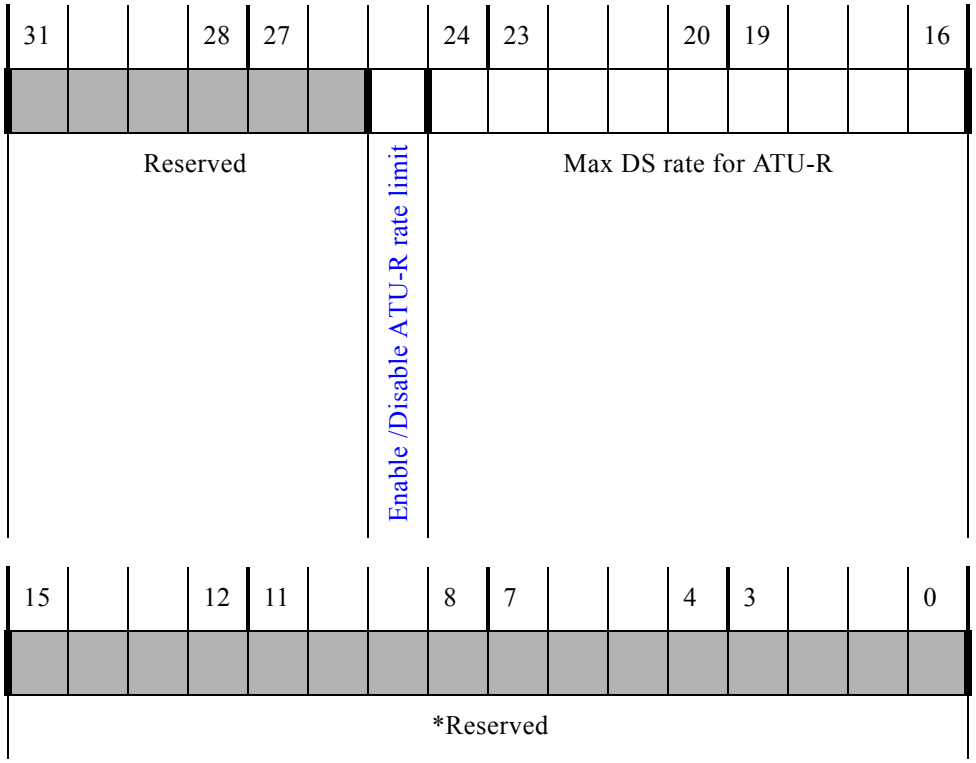
***This bit is reserved for Anaconda/Diamondback/Eagle Operation**

Figure 67. OTPN.930 (offset 6)

Table 47 OPTN.atm_fifo (offset 7)

Bits	Name	Description
15:0	*Reserved	0 Default. Note: Bits 15:0 of OPTN.ATM_fifo (offset 7) are no longer assigned to 'Tx/Rx Fast and Intl Paths'. (Similar functionality in CMV OPTN.atm_fifo_new (offset 15) bits 0-28)) They are reserved bits for Anaconda/Diamondback/Eagle.
24:16	Max DS rate for ATU-R (ATU-R only)	If Bit 25 is 1, Bits 24-16 define the Max DS rate that the ATU-R would like.
25	Enable/ Disable ATU-R rate limit. (ATU-R only)	0 Disable DS rate limit. (Default) 1 Enable DS rate limit.

***These bits are reserved for Anaconda/Diamondback/Eagle Operation**



***These bits are reserved for Anaconda/Diamondback/Eagle Operation**

Figure 68. OPTN.atm_fifo (offset 7)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 48 OPTN.lpbk_config (offset 13)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
OPTN.1pbk_config **Description:** Set up general Loopback features such as ATM addresses, UTOPIA level, Tx mode, ADSL and ATM scrambling. (Refer to ANCMV-05)	13	1	ATU-C ATU-R

Bits	Name		Description
7:0	Fast path ATM address		Default is 2, the same value used for Tx and Rx address. Unused in UTOPIA Level 1 mode.
15:8	Intl path ATM address		Default is 1, the same value used for Tx and Rx address. Unused in UTOPIA Level 1 mode.
16	Interleaver off or on	0	Interleaver off. (default)
		1	Interleaver on and interleaver depth is **8**
20	UTOPIA Level	0	UTOPIA Level 1 (default)
		1	UTOPIA Level 2
21	Tx Mode	0	Cell Tx mode (default. Always cell mode in UTOPIA Level 2, regardless of settings)
		1	Octet Tx mode. (only valid in UTOPIA Level 1 mode)
24	ADSL Scrambling	0	ADSL scrambling on. (default)
		1	ADSL scrambling on.
25	ATM Scrambling	0	ATM scrambling on. (default)
		1	ATM scrambling on.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

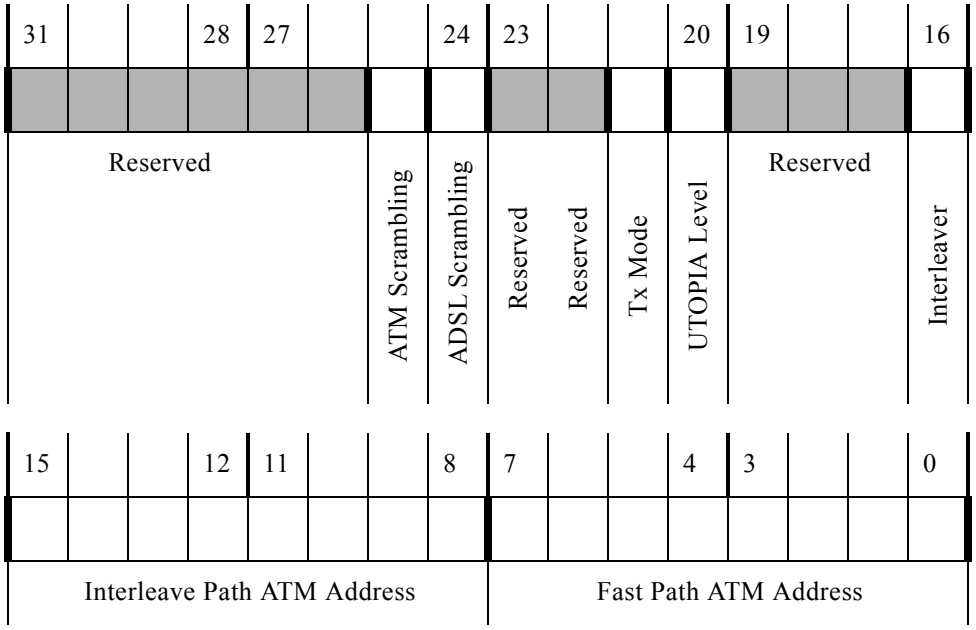


Figure 69. OPTN.lpbk_config (offset 13)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 49 OPTN.1pbk_rate (offset 14)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
OPTN.1pbk_rate **Description:** Set up Fast and intl latency path rates in Loopback mode. (Refer to ANCMV-05)	14	1	ATU-C ATU-R

Bits	Name	Description
7:0	Fast path data rate	Sets Fast path data rate. (defaults to 0)
15:8	Intl path data rate	Sets Intl path data rate. (defaults to **0xB4**, 180 decimal).

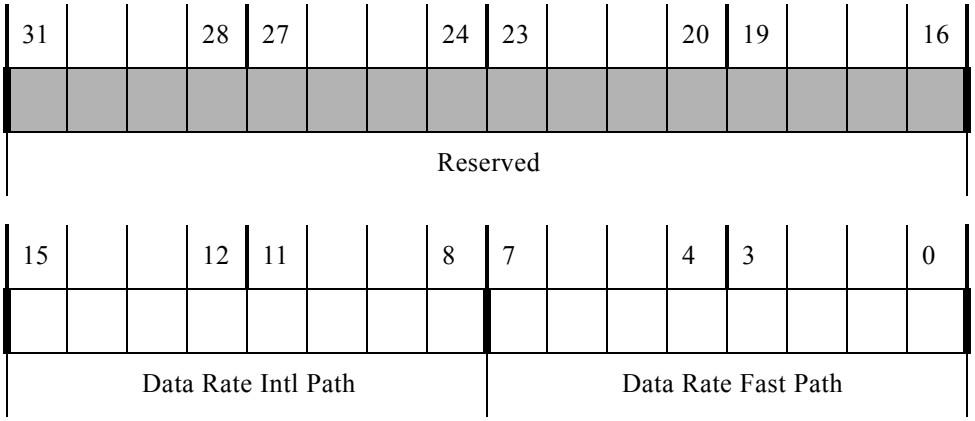


Figure 70. OPTN.1pbk_rate (offset 14)

Table 50 OPTN.atm_fifo_new (offset 15)

(Anaconda/Eagle/Diamondback Specific CMV)

Name	O	L	Access
OPTN.atm_fifo_new **Description:** This sets up the Tx and Rx FIFO sizes in each latency path. Default value is **0x02020202** (Refer to ANCMV-05)	15	1	ATU-C ATU-R

Bits	Name	Description
4:0	Rx FIFO size Fast Path	Defaults to 9 ATM cells. Min = 2
12:8	Rx FIFO size Intl Path	Defaults to 9 ATM cells. Min = 2
20:16	Tx FIFO size Fast Path	Defaults to 9 ATM cells. Min = 2
28:24	Tx FIFO size Intl Path	Defaults to 9 ATM cells. Min = 2
29	Discard_cell_HEC	0 Discard cells with bad HEC. (default) 1 Do not discard cells during bad HEC.
30	Discard_cell_presync	0 Discard cells during pre-sync state (default) 1 Do not discard cells during pre-sync state.
31	Discard_cell_unassigned	0 Discard unassigned cells. (default) 1 Do not discard unassigned cells.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

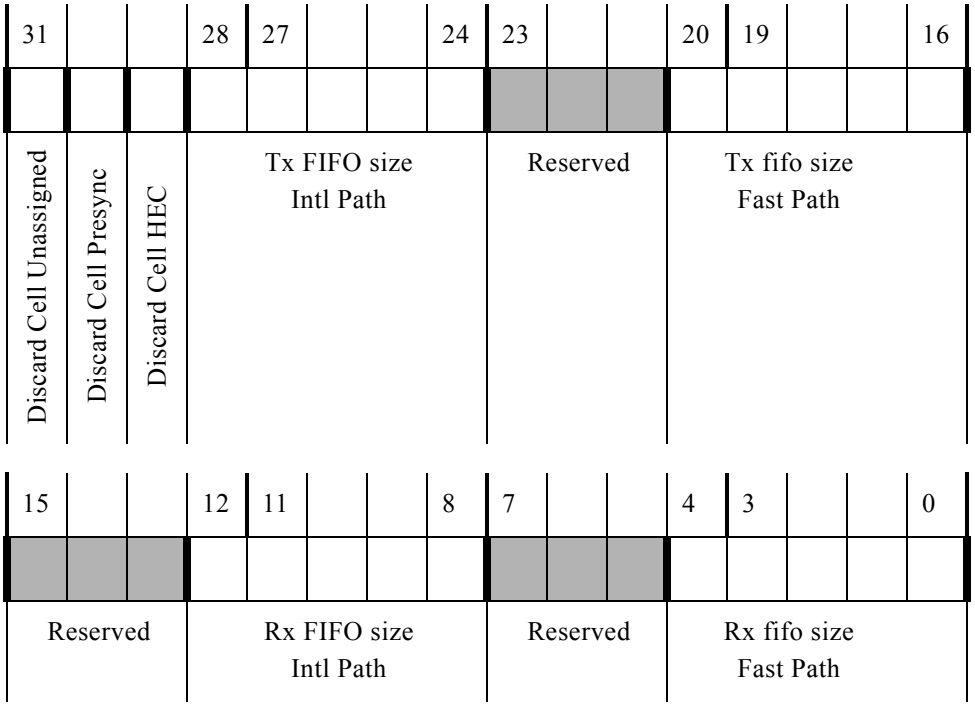


Figure 71. OPTN.atm.fifo_new (offset 15)

Usage

OPTN.options (OPTN offset 0)

OPTN.options is used to identify whether the Echo Canceller (EC), Trellis-coded Modulation (TCM), and Frequency Domain Equalization (FDQ) Adaption options are available. If they are, the ME can select or deselect their use.

OPTN.options may also be used to change the PGA setting. The value entered as an offset will be subtracted from the nominal PGA cutback value, which is 6 dB at the ATU-C and 3 dB at the ATU-R.

For example, if you enter the value “110” into this field at the ATU-C, the AD20MSP918 will remove 6 dB from the nominal PGA cutback, so that the cutback will now be 0 dB. The PGA gain will now be 6 dB higher than nominal.

This feature should improve performance over links with bridge taps. However, if you lower PGA cutback, you should set the interleave depth to the maximum allowed to avoid errors due to clipping.

For further OPTN CMV information regarding Multiport operations, please refer to the Anaconda/Diamondback/Eagle CMV Overview Section in this manual.

When the modem is using coding, the datapath, due to coding gain, will have a higher margin than the path that is not being used for data. For rate-adaptive links, this means that the Interleave Path, which is used for data, typically has a higher margin than the Fast Path.

For example, on a typical rate-adaptive link with coding, the ME will set the desired margin to 1 or 2 dB. The coding gain will cause the effective margin on the Interleave Path to be about 6 dB, but the Fast Path, which is not coded, will still have a margin of about 1 dB. This discrepancy can cause fast-path errors, which in turn can cause problems with the EOC channel and with the indicator bits, which are transmitted over the fast path.

To address this problem, bit 11 of OPTN.options (Offset 0) allows the ME to set the fast-path margin for rate-adaptive links. When this bit is set, the AD20MSP918 will set the margin to 6 dB, which should reduce the number of fast-path errors.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

One drawback of the above feature is that it may cause problems with links over very long loops. Under these conditions, it may not be possible to provide the 6 dB margin required for the Fast Path, but it may be able provide the 1 dB margin required for the Interleave Path. In this case, the AD20MSP918 would fail to link even though adequate data communication performance were possible.

To avoid this problem, the ME should leave bit 11 cleared (the default), which will set the fast-path margin to the value entered into the ADPT CMV (again, typically 1 or 2 dB). The AD20MSP918 would then be able to close the link, but the EOC and indicator bits would be susceptible to errors.

Bit 11 is only used for rate-adaptive links; it is not used for explicit-rate links.

The Network Timing Reference (NTR) is an 8 KHz clock signal present at the ATU-C. Use requires enablement at both ATU-C and ATU-R from the ME-C and ME-R.

OPTN.utopia (OPTN offset 2)

OPTN.utopia defines parameters for configuring the ATM/UTOPIA interface. The default setting for ATM, 0x01500000, results in the following default system characteristics:

Anaconda/Diamondback	**Eagle**
ATM Mode	ATM Mode
SCLAV Mode	MCLAV Mode
MPHY Mode	SPHY Mode
Framing Mode 3	Framing Mode 1
Cell Mode	Cell Mode
DS MFC Enabled	Default: 0x01500000 (same as 918/930)
Default: 0x23200000	

Note:

a) CLAV0 Mapped to INTL Path at the ATU-C, (not applicable for Anaconda/Eagle).
b) "Use CLAV1" at the ATU-R, (not applicable for Anaconda/Eagle)

Level 1 UTOPIA has no meaning for Anaconda/Diamondback products. They are by definition "Multiport" products and are required to operate in UTOPIA Level 2. Because 1 CLAV per port is not available, these products operate with UTOPIA Level 2 Address Polling, not direct status indication.

For more information about configuration of the ATM/UTOPIA interface and using it in TEST-LOOPBACK, refer to ANCMV-05.

OPTN.930 (OPTN offset 6)

The 930 CO and 930 RT modems can be in one of two modes, ”normal” or “standby” mode. In “normal” (or operational) mode the modem is ready for link initialization. “Standby” mode link has been added to make use of circuitry in the AD6440 and the AD8016 Tx driver that allow them to enter states with lower quiescent currents. While the 930 CO or the 930 RT is in “standby” mode, link initialization is not possible.

Writing ‘OxC’ to CNTL offset 0 will place in the modem (“normal” or “standby”) indicated by bit 4 of OPTN offset 6. The current mode of system operation (“normal” of “standby”) is always reflected in bit 4 of STAT offset 3.

At power-up or reset the 930 CO and the 930 RT default to normal mode.

Prior to placing the modem in “standby” mode, the modem should be reset. The modem can be brought out of “standby” mode and into “normal mode either by using the combination of OPTN offset 6 and CNTL offset 0 or by issuing another reset.

On the CO 1T reference design, in “normal” mode the AD6440 pin ‘EXT_DRV_D’ (pin 45) drives PWDNO (AD8016 driver input pin) high. Since the ‘PWDN1’driver input pin is pulled to ground externally in the reference design, the following truth table shows how the selected mode (“normal” of “standby”) corresponds to the AD8016 Tx driver state.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

	PWDN1	PDWN0
Standby	0	0
Normal	0	1

On the RT 1T reference design, in "normal" mode the AD6440 pin 'EXT_DRV_D' (pin 45) drives PWDNO (AD8016 driver input pin) high. The following truth table shows how the selected mode ("normal" or "standby") corresponds to the AD8016 Tx driver state.

	PWDN1	PDWN0
Standby	0	0
Normal	1	1

OPTN.atm_fifo (OPTN offset 7, bits 15:0)

The ME needs to configure the Tx ATM FIFO and Rx ATM FIFO of an AD6438/6449 to ensure a continuous flow of data in the ATM network. These rules apply:

1. The number of ATM cells allocated on the Fast Path plus the number of cells allocated on the Interleaved Path should never exceed a total of eight.
2. If the ME does not specify the number of cells allocated to both paths, (i.e. leaves bits 15:0 set to the default of '0'), the default configuration will be set to 4 and 4.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Notes

1. After a reboot, the ME has one second to send an OPTN before the ATU-R goes into initialization.
2. OPTN.cpr_01 (OPTN offset 5) allows you to turn off the default constraint against data rates that are multiples of 128 Kbps, and to enable or disable the software workaround for those rates.

   The constraint was necessary because of a condition in the AD6439. When the total number of bytes transferred across the DME-DTIR interface is a multiple of four, the resultant link may exhibit constant CRC errors. You can use either the default constraint against the data rates (Bit 8) or the software workaround (Bit 9). We suggest you set both bits.
3. Bits 15:0 are reserved for Anaconda/Diamondback operation. Similar functionality can be found in CMV OPTN.atm_fifo_new (offset 15, bits 28:0).

Related CMVs

None.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

PFCL (Profile Control)

Summary

Name	O	L	Access	Description
PFCL.status	0	1	ATU-C R-only ATU-R R-only	Returns a dataword stating the training profile currently in use for near-end Rx and Tx, and the number of fast retrains executed so far.
PFCL.control	1	1	ATU-C R/W ATU-R R/W	Sets the fast retrain margin to be used during profile selection.

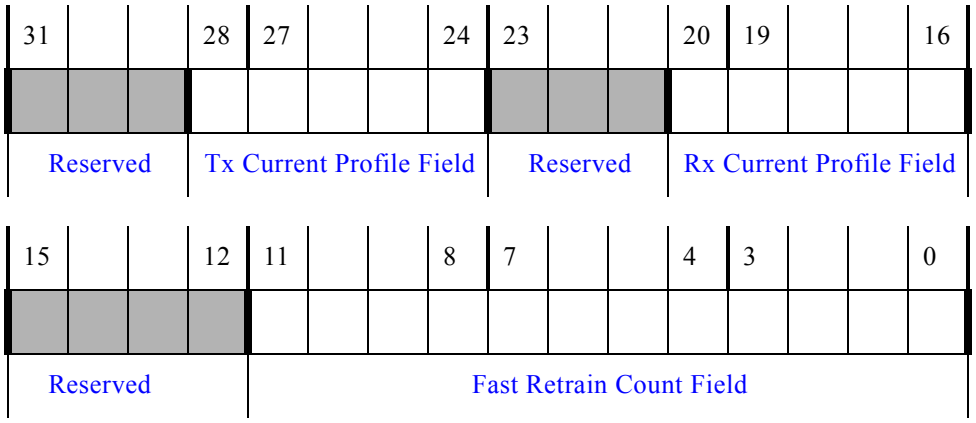


Figure 72. PFCL.status (offset 0)

Table 51 PFCL.status (offset 0)

Bits	Name	Description
11:0	Fast Retrain Count	The number of successful fast retrains since the last full-length Lite-mode train. The ATU resets this counter after 4096 times or after a reboot. (When count reaches 4095)
20:16	Rx Current Profile	The number of the profile currently in effect for near-end Rx, in hexadecimal. These other values apply: 0x1F There has been no Rx profile selection yet. 0x10 Rx profile selection failed. This value (0 X 10) is preserved during the subsequent full train, until the newly chosen tx/rx parameters are saved as a new profile.
28:24	Tx Current Profile	The number of the profile currently in effect for near-end Tx, in hexadecimal. These other values apply: 0x1F There has been no Tx profile selection yet. 0x10 Tx profile selection failed. This value (0 X 10) is preserved during the subsequent full train, until the newly chosen tx/fx parameters are saved as a new profile.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 52 PFCL.control (offset 1)

Bits	Name	Description
3:0	Fast Retrain Margin Field	The fast retrain margin, in dB, range 0-15.
15:12	Fast Retrain Trigger	This value left-shifts the FR trigger threshold. A higher number means less sensitivity.

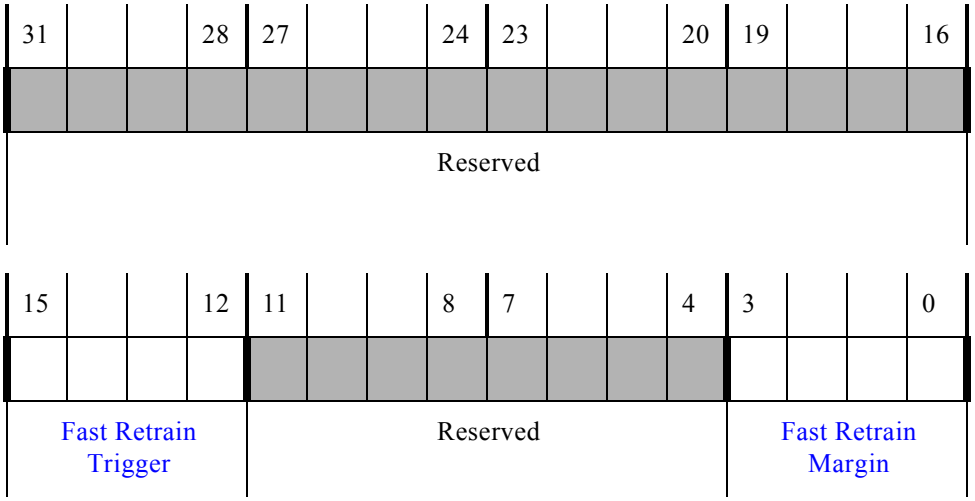


Figure 73. PFCL.control (offset 1)

Usage

Introduction

A profile is a set of Rx or Tx characteristics that the modem uses. It stores the profile when completing the first successful fast retrain after a full-length Lite-mode train.

The modem can store up to 8 different profiles. On every subsequent retrain, it selects one of these profiles for use. A counter records the number of fast retrains. It gets reset when the modem stores a profile again. If all eight profiles have been used up, the modem writes the new profile over the least-used profile.

You can influence the profile selection process by writing the value of the Lite-mode SNR margin to be used in the profile selection process during the next fast retrain. You use PFCL.control (Offset 1) for this purpose before starting a fast retrain or a full-length Lite-mode link. That value will prevail throughout the full-length Lite-mode link or until you change it.

You can also configure with PFCL.control prior to starting a fast retrain; in that case, the value will prevail through the next fast retrain, and will remain through subsequent bit retrains until you change it.

The modem stores PFCL.status and PFCL.control as part of the profile information. When it restores the profile, it also restores the PFCL values that existed when the profile originally was stored.

The Concept of “Lite SNR Margin”

During a fast retrain, for each stored profile, the firmware does a bin-by-bin comparison of the profile’s SNR requirements with the SNRs attained during that fast retrain. This comparison takes two margin values into account: the desired SNR margin (selected in ADPT) and the lite SNR margin (selected in PFCL.control, Offset 1).

The firmware subtracts the desired SNR margin from the SNRs measured during the last fast retrain and uses the differences to select a profile. In the case of a lite SNR margin of zero, the rule is, that for every bin,

(Measured SNR - Desired SNR margin) - Required Profile SNR) > 0

In the case of non-zero lite SNR margin values, the firmware inspects each profile and subtracts the lite SNR margin from the profile SNR requirements. Doing this actually reduces the SNRs that need to be attained during a fast retrain across all bins by an amount equal to the lite margin. The rule is, that for every bin,

(Measured SNR - Desired SNR Margin) - (Required Profile SNR - Lite SNR Margin) > 0

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Lite SNR margin actually relaxes the profile selection criteria, but it can also increase the possibility of a mismatch between a profile and the current line conditions. Changing the lite margin may result in an auto reboot and subsequent full-length lite train.

Clearing Profiles

To clear the profiles currently in FLASH, set bit 20 in OPTN.options (Offset 0) on either the ATU-C or the ATU-R prior to starting a full-length Lite-mode link. Once a modem is in OPERATIONAL, the profiles will be cleared by a background task. This should complete within 1-2 seconds, during which time fast-retrain initiation will be disabled.

Related CMVs

OPTN.options (OPTN offset 0) for Lite Mode

Bits 25:20 allow the ME to control fast retrain functionality, including profile clearing.

PFRX

Retrieves information about the Rx profile's usage.

PFTX

Retrieves information about the Tx profile's usage.

STAT.status (STAT offset 0)

Bits 14 and 29 report some information related to profiles. Bits 11:8 return a value of 0x7 if the ATU is in FAST RETRAIN state.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

PFRX (Rx Profile)

Summary

Name	O	L	Access	Description
PFRX.profilenum	0-7	8	ATU-C R-only ATU-R R-only	Returns a dataword stating information about the Rx profile, the number of which is equal to the offset.

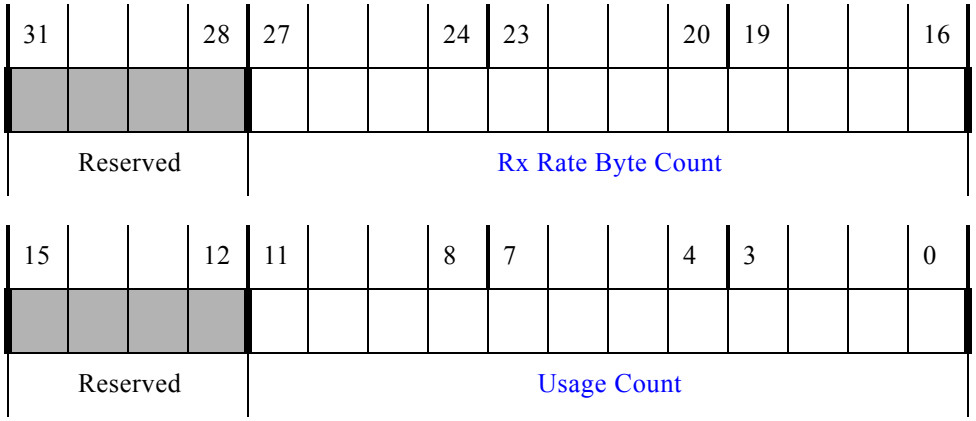


Figure 74. PFRX.profilenum (offsets 0-7)

Usage

PFRX provides information on the rate associated with a given Rx profile and a record of the number of times it has been autoselected since its last reboot or auto reboot.

Notes

None

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Related CMVs

OPTN.options (OPTN offset 0) for Lite Mode

Bits 25:20 allow the ME to control profiling.

PFCL

Finds out which Tx and Rx profiles are in use, counts the number of fast retrains so far and sets the fast retrain margins.

PFTX

Retrieves information about the Tx profile's usage.

STAT.status (STAT offset 0)

Bits 14 and 29 report some information related to profiles. Bits 11:8 return a value of 0x7 if the ATU is in FAST RETRAIN state.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

PFTX (Tx Profile)

Summary

Name	O	L	Access	Description
PFTX.profilenum	0-7	8	ATU-C R-only ATU-R R-only	Returns a dataword stating information about the Tx profile, the number of which is equal to the offset.

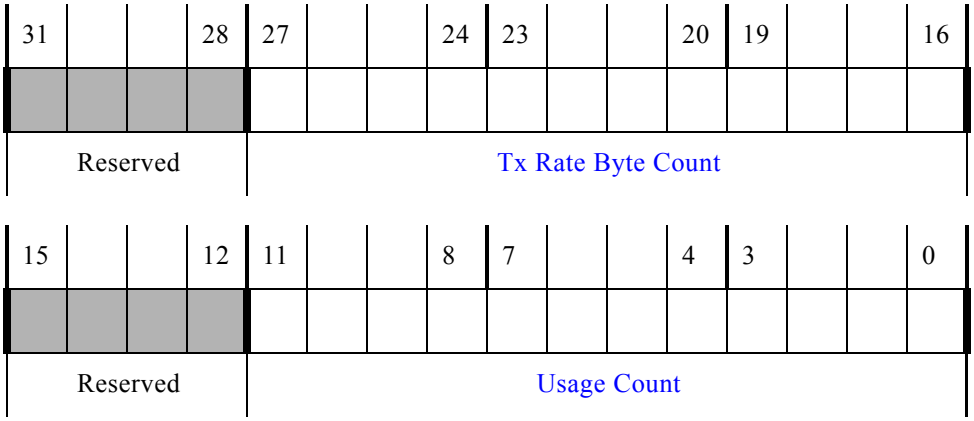


Figure 75. PFTX.profilenum (offsets 0-7)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 53 PFTX.profilenum (offsets 0-7)

Bits	Name	Description
11:0	Usage Count	The number of times this profile was selected on retrain. The modem resets it after 4096 times. (When count reaches 4095)
27:16	Tx Rate Byte Count	The Tx profile receive-rate byte capacity, including • payload, • overhead, • checkbytes for Tx Fast Path, • checkbytes for Tx Interleave Path. A value of zero denotes that the profile was not used.

Usage

PFTX provides information on the rate associated with a given Tx profile and a record of the number of times it has been autoselected since its last reboot or auto reboot.

Notes

None

Related CMVs

OPTN.options (OPTN offset 0) for Lite Mode

Bits 25:20 allow the ME to control profiling.

PFCL

Finds out which Tx and Rx profiles are in use, counts the number of fast retrains so far, and sets the fast retrain margins.

PFRX

Retrieves information about the Rx profile's usage.

STAT**.status (STAT offset 0)**

Bits 14 and 29 report some information related to profiles. Bits 11:8 return a value of 0x7 if the ATU is in FAST RETRAIN state.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

PSDM (Power Spectral Density Mask)

Summary

Name	O	L	Access	Description
PSDM.config	0	1	ATU-C R/W	Restricts ATU-C output power to a new maximum PSD. Default: 0x23C60000
			ATU-R R/W	Restricts ATU-R output power to a new maximum PSD. Default: 0x00003A4C
PSDM.actual	1	1	ATU-C R-only	Reads the PSD currently in effect at the ATU-C. Default: 0x23C60000
			ATU-R R-only	Reads the PSD currently in effect at the ATU-R., and shows the transmit PSD during C-reverb1. Default: 0x00003A4C

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

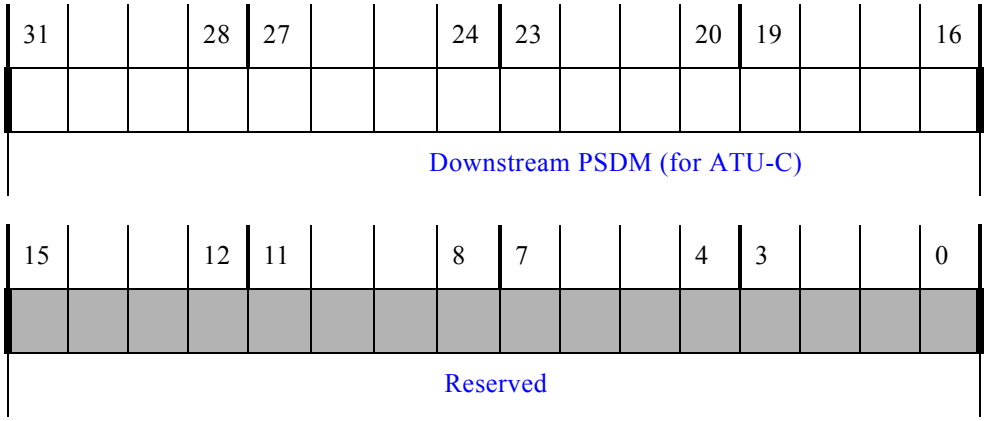


Figure 76. ATU-C PSDM.config (PSDM offset 0) and PSDM. actual (PSDM offset 1

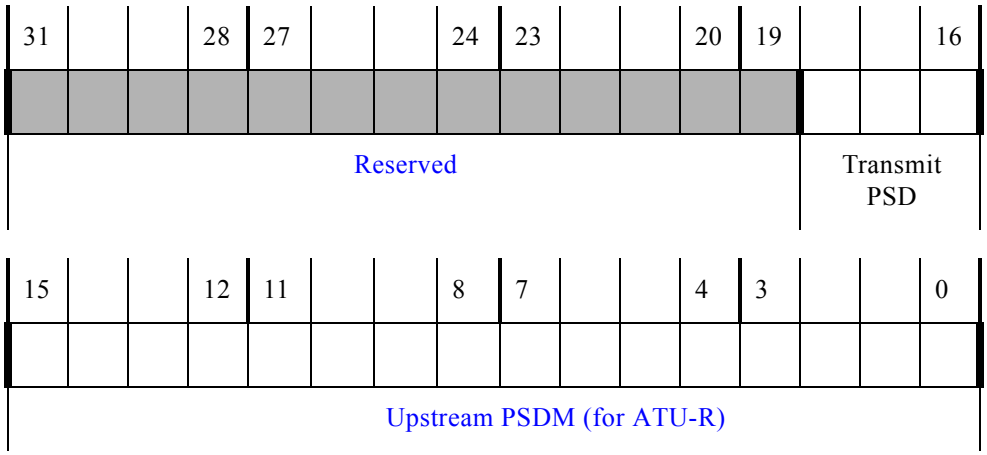


Figure 77. ATU-R PSDM.config (PSDM offset 0) and PSDM. actual (PSDM offset 1)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

PSDM.config (Offset 0) allows an ME to restrict ATU output power to a desired maximum power spectral density (PSD). The ME-C sets or reads the DS PSDM at the ATU-C and the ME-R sets or reads the US PSDM at the ATU-R.

The nominal value for PSDM at the ATU-C is 0x23C6, which corresponds to -40 dBm/Hz. The nominal value for PDSM at the ATU-R is 0x3A4C, which corresponds to -38 dBm/Hz.

PSDM.actual (PSDM offset 1) gives the actual PSD used for the link in both the upstream and downstream directions. The format of the PSDM.actual CMV word is identical to that of the PSDM.config CMV word described above.

PSDM (offset 1) field on the RT (bits 16-18) shows the transmit PSD during C-reverb1 encoded in C-Msg1. This is RT only and Read only.

Example 1

To increase the DS power by 2dB, the PSDM.config (PSDM offset 0) at the CO should be set up as follow:

$$2\text{dB} = 20 \times \log \left[\frac{\text{PSDMconfig}}{0\text{x}23\text{C}6} \right]$$

$$\Rightarrow \text{PSDMconfig} = \left[\text{Log}^{-1}\left(\frac{2}{20}\right) \right] \times (0\text{x}23\text{C}6) = 0 \times 2\text{D}09$$

Example 2

To decrease the US power by 3dB, the PSDM.config (PSDM offset 0) at the RT should be set up as follows:

$$-3\text{dB} = 20 \times \log\left[\frac{\text{PSDMconfig}}{0\text{x}3\text{A}4\text{C}}\right]$$

$$\Rightarrow \text{PSDMconfig} = \left[\text{Log}^{-1}\left(\frac{-3}{20}\right)\right] \times (0 \times 3\text{A}4\text{C}) = 0 \times 2945$$

Notes

In Lite Mode, using escape to fast retrain may result in application of a PSDM greater than that specified in PSDM.config (PSDM offset 0). To avoid this behavior, escape to fast retrain should be disabled in OPTN offset 4.

Related CMVs

None.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

RATE

Summary

Name	O	L	Access	Description
RATE.actual	0	1	ATU-C R-only ATU-R R-only	Returns the current US and DS data rates in bytes per symbol.
RATE.maximum	1	1	ATU-C R-only ATU-R R-only	Returns the maximum possible data rates.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 54 RATE.actual (offset 0)

Bits	Name	Description
7:0	US	The number of data bytes per DMT symbol actually being transmitted on the US link.
24:16	DS	The number of data bytes per DMT symbol actually being transmitted on the DS link.

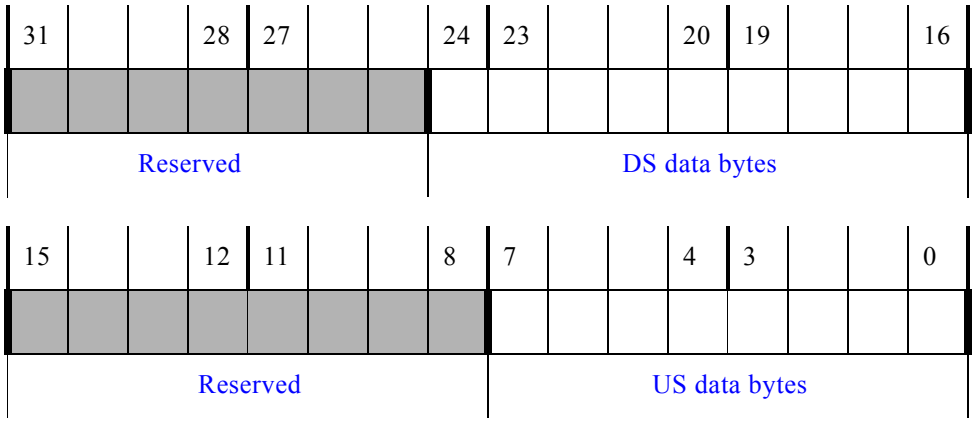


Figure 78. RATE.actual (offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 55 RATE.maximum (offset 1)

Bits	Name	Description
7:0	Maximum US	The maximum number of upstream data bytes (including overhead and parity) per DMT symbol.
24:16	Maximum DS	The maximum number of upstream data bytes (including overhead and parity) per DMT symbol.

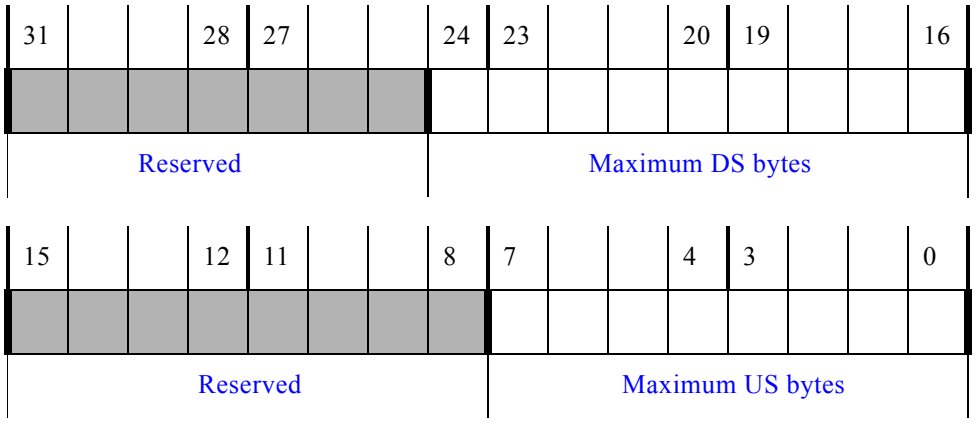


Figure 79. Rate.maximum (offset 1)

Usage

RATE.actual (RATE offset 0) is supported for both Explicit-rate and Rate-Adapted configurations.

RATE.actual is the number of payload bytes per symbol on the US and DS data paths.

RATE.maximum (RATE offset 1) represents the maximum upstream or downstream capacity that is achievable, given the measured SNR on each tone. The capacity includes overhead and parity bytes.

The data rates are specified in data bytes per DMT symbol. The DMT symbol rate is 4000 Hz, so that the data rate has a 32 Kbit granularity. As an example, if bits 7:0 (msb to lsb) are 0x0A, then the data rate is

10 * 8 * 4000 = 320 Kbps.

Notes

None.Related CMVs

ADPT

DOPT, UOPT

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

RXDA (Receive Data)

Summary

Name	O	L	Access	Description
RXDA.data	1-2	2	ATU-C R-only ATU-R R-only	Receives a message transmitted over the EOC from a TXDA.data.
RXDA.Clear_EOC	10	1	ATU-C R-only ATU-R R-only	Receives a message transmitted over the EOC from a TXDA.Clear_EOC.
RXDA.mailbox	11	1	ATU-C R/W ATU-R R/W	Notifies the recipient ME that a message is in RXDA.data.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 56 RXDA.data (offset 1)

Name	O	L	Access
RXDA.data **Description:** Receives a message transmitted over the EOC from a TXDA.data.	1	2	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	RXDA.data	Actual data received

All 64 bits of RXDA.data (offsets 1 and 2) hold the EOC message.

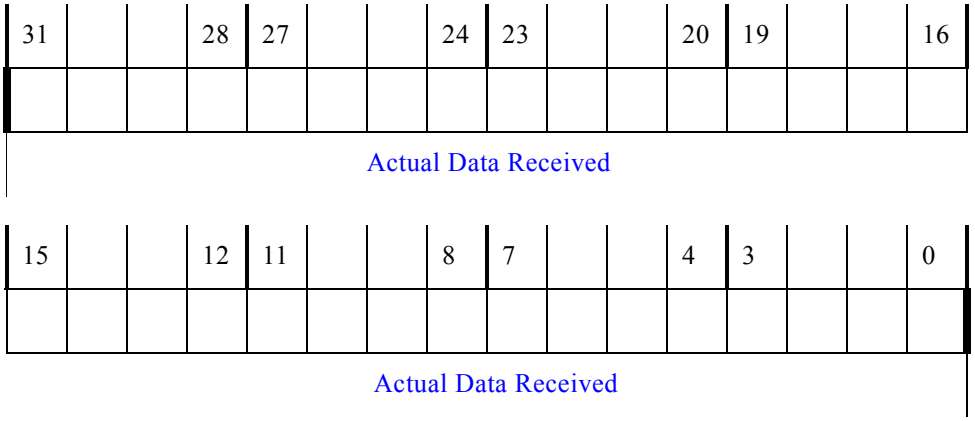


Figure 80. RXDA.data (offset 1)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 57 RXDA.data (offset 2)

Name	O	L	Access
RXDA.data **Description:** Receives a message transmitted over the EOC from a TXDA.data.	2	2	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	RXDA.data	Actual data received

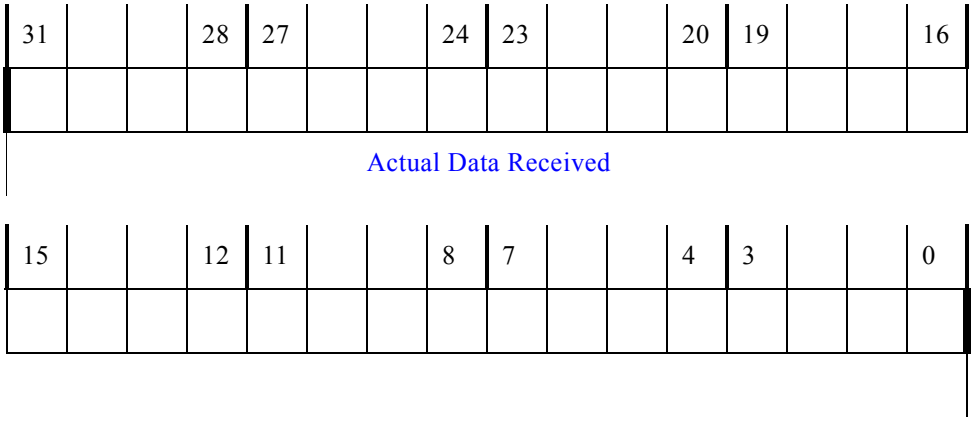


Figure 81. RXDA.data (offset 2)

Table 58 RXDA.Clear_EOC (offset 10)

Name	O	L	Access
RXDA.Clear_EOC **Descrip-tion:** Receives a message transmitted over the EOC from a TXDA.Clear_EOC.	10	1	ATU-C R-only ATU-R R-only

Bits	Name	Description
31:0	RXDA.Clear_EOC	Actual data received

31			28	27			24	23			20	19			16

Actual Data Received

15			12	11			8	7			4	3			0

Actual Data Received

Figure 82. RXDA.Clear_EOC (offset 10)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 59 RXDA.mailbox (offset 11)

Name	O	L	Access
RXDA.mailbox **Description:** Notifies the recipient ME that a message is in RXDA.data.	11	1	ATU-C R/W ATU-R R/W

Bits	Name	Description
0	RXDA.mailbox	Notifies the recipient ME that a message is in RXDA.data.
23:16	Number of bytes received	Displays number of bytes received

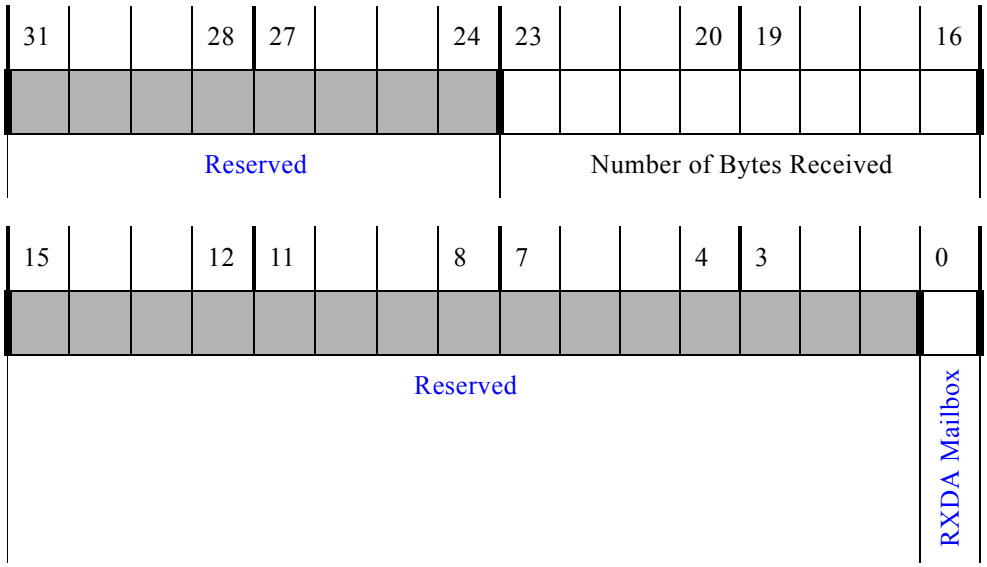


Figure 83. RXDA.mailbox (offset 11)

A set RXDA mailbox Bit means that a message is available in RXDA.data (Offsets 1-2). A cleared bit means no message is there. Furthermore, if RXDA mailbox is clear then RXDA.data should not be read because a mailbox transfer maybe in progress.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

Introduction

RXDA can only be used in conjunction with TXDA.

There are two TXDA.data CMVs and two RXDA.data CMVs. A message to be transferred is contained in two 32-bit words, TXDA.data on transmission and RXDA.data on receipt.

Sending a Downstream Message

To send a downstream message,

1. The ME-C checks the ATU-C TXDA Mailbox Bit (TXDA.mailbox, Offset 11, bit 0). If it is set, the ME-C must wait. If it is clear, the ME-C goes on to the next step.
2. The ME-C writes the message data in TXDA.data (Offsets 1-2) at the ATU-C. It need not specify the length of the message.
3. The ME-C begins the transmission by writing a one in the TXDA Mailbox Bit.
4. The ATU-C automatically transmits the data to RXDA.data (RXDA offsets 1,2) of the ATU-R, sets the RXDA Mailbox Bit (RXDA.mailbox, Offset 11, bit 0) and clears the TXDA Mailbox Bit.
5. The ME-R discovers that the message is there. It can do this by polling the ATU-R's RXDA Mailbox Bit, or with a FLAG.mask (FLAG offset 0).
6. The ME-R reads the message and clears the ATU-R's RXDA Mailbox Bit.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Sending an Upstream Message

To send an upstream message,

1. The ME-R checks the ATU-R TXDA Mailbox Bit (TXDA.mailbox, Offset 11, bit 0). If it is set, the ME-R must wait. If it is clear, the ME-R goes on to the next step.
2. The ME-R writes the message data into the TXDA.data (TXDA offsets 1-2) at the ATU-R.
3. The ME-R requests transmission by writing a one in the TXDA Mailbox Bit (TXDA.mailbox, Offset 11, bit 0).
4. The ATU-C continuously polls the TXDA Mailbox Bit at the ATU-R, as long as its own RXDA Mailbox Bit is clear. The ATU-C will not overwrite a message in its RXDA.data.
5. When the ATU-C finds the ATU-R's TXDA Mailbox Bit set, it reads the ATU-R's TXDA.data[] into its own RXDA.data.
6. Upon completion, the ATU-C sets its own RXDA Mailbox Bit and the ATU-R clears its own TXDA Mailbox Bit.
7. The ATU-C suspends polling the ATU-R TXDA Mailbox Bit until the ME-C clears the RXDA Mailbox Bit.
8. The ME-C must detect the ATU-C's RXDA Mailbox Bit being set. It can do so by polling or via the Flag Line.
9. On detecting a message, the ME-C reads it.
10. The ME-C clears the ATU-C's Mailbox Bit.

Note: Please refer to application note ANCMV-04

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Notes

An ME can configure an ATU to set the PF4 flag when an RXDA Mailbox Bit indicates that a message has been received. See FLAG for a description of this configuration.

Related CMVs

FLAG

Programs the ATU to trigger the Flag Signal when specified events occur. The Mailbox Bit being set is such an event.

INFO

Returns information identifying the ATU-C or ATU-R. You can use the Mailbox Bit to cause the ATU-C to send one automatically to the ATU-R.

TXDA

Used in conjunction with RXDA.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

STAT (Status)

Summary

Name	O	L	Access
STAT.status **Description:** Requests return of an ATU status dataword.	0	1	ATU-C, ATU-R R-only
STAT.initialization_failure_codes **Description:** Requests initialization failure code.	1	1	ATU-C, ATU-R R-only
STAT.930 **Description:** Select between normal mode or standby mode.	3	1	ATU-C, ATU-R R-only
STAT.lpbk_rate **Description:** This reflects the actual fast and intl latency path rates in the UTOPIA loopback mode. The firmware will override invalid user settings in OPTN. lpbk_rate with valid defaults	4*	1	ATU-C, ATU-R R-onl;y
STAT.atm_fifo **Description:** This reflects the actual Tx and Rx FIFO sizes in each latency path. The firmware will override invalid user settings in OPTN.atm_fifo with valid defaults	5*	1	ATU-C ATU-R

***Anaconda/Diamondback/Eagle Specific CMV**

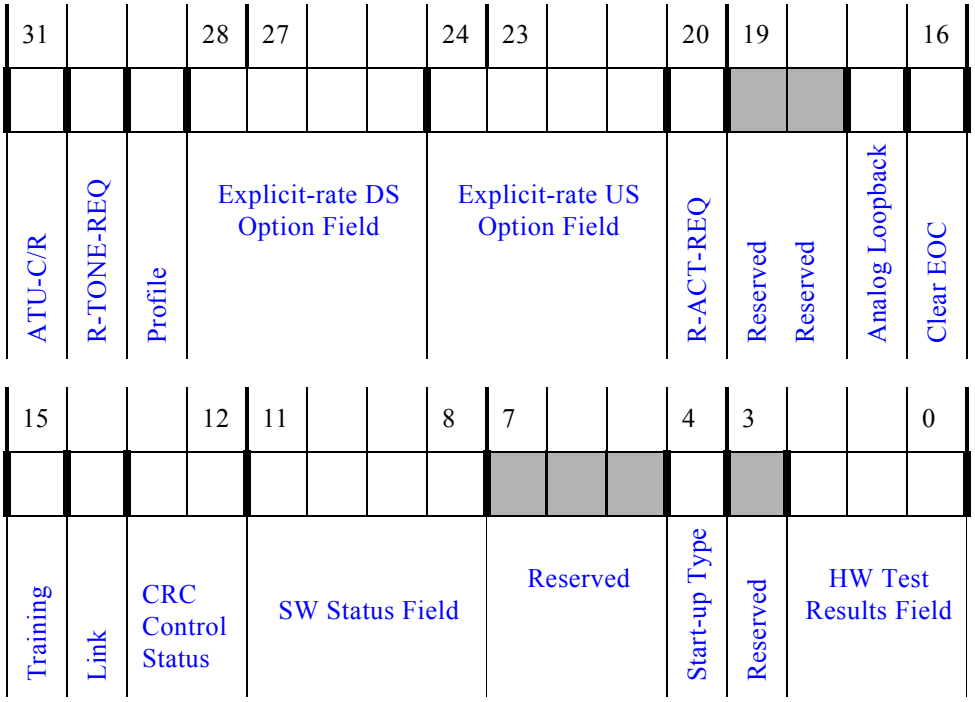


Figure 84. ATU-C STAT.status (STAT offset 0)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Figure 85. ATU-R STAT.status (STAT offset 0)

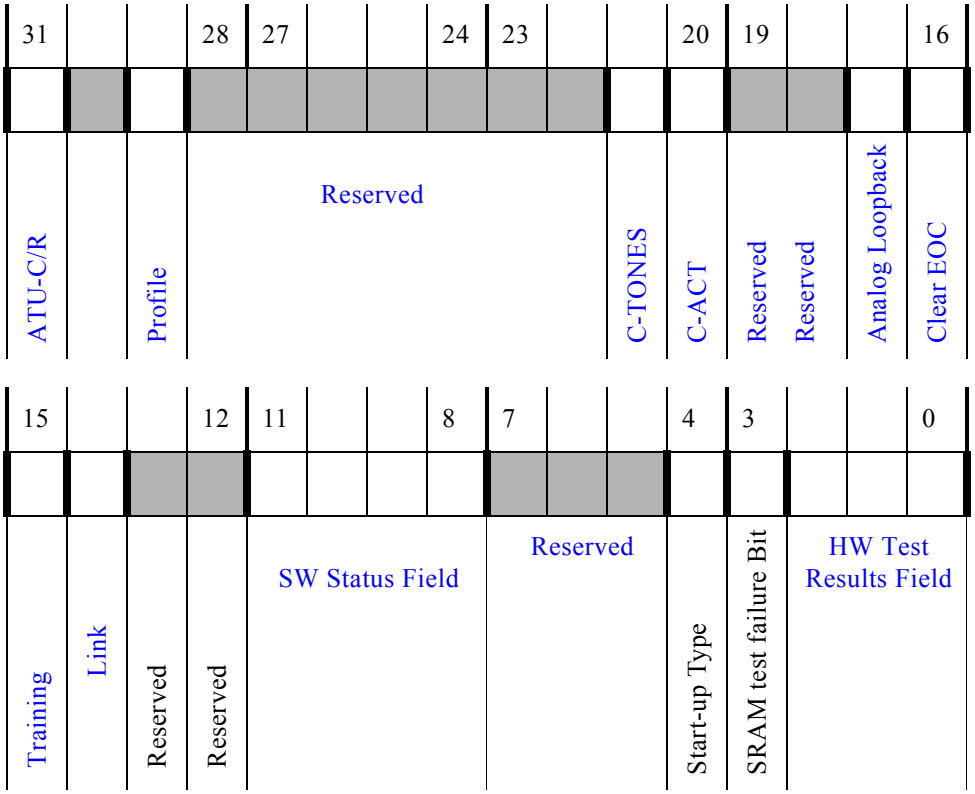


Table 60 STAT.status (offset 0)

Bit	Name			Description
0	HW Sta-tus Bit.	2		Indicates the overall results of the diagnostic tests (as set up with TEST and CNTL). 0 - All test passed. 1 - One or more tests failed.
1	AD6439 Status Bit.			Indicates the overall results of the AD6439 register test. 0 - All test passed. 1 - One or more tests failed.
2	AD6438 Status Bit.			Indicates the overall results of the AD6438 register test. 0 - All test passed. 1 - One or more tests failed.

Table 60 STAT.status (offset 0)

Bit	Name			Description
3	Interleave RAM Status Bit.			Indicates the result of the Interleave RAM test. 0 - All tests passed. 1 - One or more tests failed.
4	Startup Type			Indicates the standard defining the startup. 0 - T1.413 1 - G.hs
7:5	Reserved			
11:8	SW Status Field			This field reports the current state of the ATU.
		Binary	**Hex**	**Description**
		0000	0x0	ATU-C in C-IDLE ATU-R in R-ACT-REQ or R-TONE-REQ
		0001	0x1	ATU is in the INITIALIZATION state.
		0010	0x2	ATU is in OPERATIONAL state.
		0011	0x3	ATU is in FAIL state.
		0100	0x4	ATU is in TEST-SIGNAL state.
		0101	0x5	ATU is in TEST-HW state.
		0110	0x6	ATU is in TEST-LOOPBACK state.
		0111	0x7	ATU is in FAST-RETAIN state.
13:12	CRC Control Status Field			Reports if bad CRCs are being sent intentionally. ATU-C only.
		Binary	**Hex**	**Description**
		00	0x0	Both links are in normal operations.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 60 STAT.status (offset 0)

Bit	Name			Description
		00	0x1	Bad CRCs are intentionally being sent in the DS
		10	0x2	Bad CRCs are intentionally being sent in the US.
		11	0x3	Bad CRCs are intentionally being sent both in the DS and US.
14	Full or Lite			0 - The modem attempted to link in Full Rate mode. 1- The modem attempted to link in Lite mode.
15	Compliant or Non-compliant Timing			0 - The modem trained with non-compliant timing (~ 20 sec). 1- The modem trained with compliant timing (~ 7 sec).
16	Clear EOC			1 - This indicates that Clear EOC is operational 0 - Clear EOC is not operational (Refer to application note ANCMV-04)
17	Analog Loopback			1 - Pass 0 - Fail Used to display the results of the integrity of channel 33 (POTS) or channel 65 (ISDN) Loopback test. (Refers to application notes ANMUM-05/ANCMV-03)
19:18	Reserved			

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 60 STAT.status (offset 0)

Bit	Name			Description
20	R-ACT- REQ (ATU-C) OR C-ACT (ATU-R)			0 - ATU-C did not detect R-ACT-REQ ATU-R did not detect C-ACT 1 - ATU-C detected R-ACT-REQ ATU-R detected C-ACT
24:21	Upstream option field (ATU-C) or C-TONES bit (ATU-R)			This field indicates which of the 4 US options was chosen. (ATU-C)
		Binary	**Hex**	**Description**
		0000	0x0	All options rejected.
		0001	0x1	Option 1 is in effect.
		0010	0x2	Option 2 is in effect.
		0100	0x4	Option 3 is in effect.
		1000	0x8	Option 4 is in effect.
				This field indicates if C-TONES were detected. (ATU-R) 0 - not detected 1 - detected
28:25	Downstream option field (ATU-C)			ATU-C only This field indicates which of the 4 DS options was chosen.
		Binary	**Hex**	**Description**
		0000	0x0	All options rejected.
		0001	0x1	Option 1 is in effect.
		0010	0x2	Option 2 is in effect.
		0100	0x4	Option 3 is in effect.
		1000	0x8	Option 4 is in effect.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 60 STAT.status (offset 0)

Bit	Name		Description
29	Profile write-error bit		This bit indicates whether there was a successful profile write at the hardware level after a fast retrain. This is for Lite mode only. 0 - Successful or no profile write. 1 - A profile write-error has occurred.
30	R-TONE-REQ (ATU-C)		ATU-C only This field indicates if R-TONES- REQ was detected. 0 - not detected 1 - detected
31	ATU-C / ATU-R bit		0 - The responent is an ATU-C 1 - The responent is an ATU-R

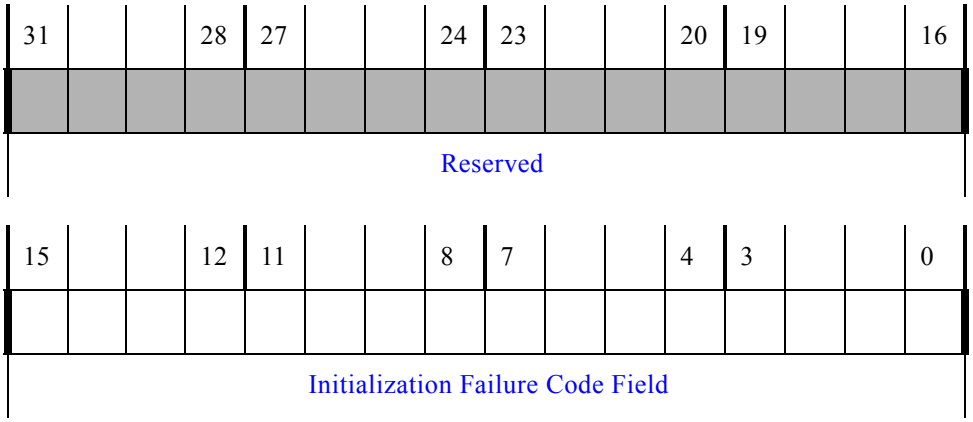


Figure 86. Return STAT.initialization_failure_codes (offset 1)

Table 61 Initialization Failure Codes

Decimal	Hex	Description
1	0x0001	CRC1_ERROR
2	0x0002	CRC2_ERROR
3	0x0003	CRC3_ERROR
4	0x0004	CRC4_ERROR
5	0x0005	CRC5_ERROR
6	0x0006	QUIET2_ERROR
8	0x0008	SEGUE1_ERROR
9	0x0009	SEQUE2_ERROR
10	0x000A	SEGUE3_ERROR
11	0x000B	SEGUE4_ERROR
12	0x000C	NEAREND_OPTION_SELECTION_ERROR
13	0x000D	SEGUE5_ERROR
18	0x0012	R_FAST_RETRAIN_RETRY_LIMIT_ERROR
19	0x0013	C_FAST_RETRAIN_RETRY__LIMIT_ERROR
20	0x0014	DEBUG_STOP
21	0x0015	REVERB3_ERROR
22	0x0016	UNUSED_STATE
23	0x0017	TIMING_MODE_SWAP_ERROR
98	0x0062	DIAG_LINK_UPLOAD_ERROR
99	0x0063	DIAG_LINK_UPLOAD_COMPLETE
100	0x0064	STAT_TIME_OUT_ERROR_RX
101	0x0065	STAT_TIME_OUT_ERROR_TX
102	0x0066	CRCRA1_ERROR

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 61 Initialization Failure Codes

Decimal	Hex	Description
103	0x0067	CRCRA2_ERROR
104	0x0068	RA_TOO_HIGH_CONFIG_ERROR
112	0x0070	RA_OPTION_SELECTION_ERROR
113	0x0071	RA_DS_MIN_RATE_NOT_SUPPORTED
114	0x0072	RA_DS_MIN_RATE_NOT_ACHIEVABLE
204	0x00CC	FAREND_OPTION_SELECTION_ERROR
300	0x012C	HS_RESTART
301	0x012D	HS_TIMEOUT
302	0x012E	HS_CLEARDOWN_ERROR
303	0x012F	HS_NO_COMMON_MODE
304	0x0130	HS_SILENCE_REQUEST
305	0x0131	HS_MESG_TOO_LONG
306	0x0132	HS_INVALID_MESSAGE
310	0x0136	C_QUIET_EF1_TIMEOUT
311	0x0137	R_QUIET_EF1_TIMEOUT
400	0x0190	ADVANCED_SWAP_TIMEOUT_ERROR
400+n	0x0191	SWAP_TIMEOUT_ERROR 401-464 401=SWAP 1, 402+SWAP 2, etc.
470	0x01D6	ADVANCE_SWAP_TIMEOUT_ERROR
600	0x0258	ADPT_DS_LAT_NOT POSSIBLE
601	0x0259	ADPT_US_LAT_NOT POSSIBLE
3537	0x0DD1	Halted at desired Tx state.
3538	0x0DD2	Halted at desired Rx state.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 61 Initialization Failure Codes

Decimal	Hex	Description
3539	0x0DD3	Halted at desired swap page.
32768	0x8000	FRCHANNEL errors placeholder
32773	0x8005	R_C_PILOT_TIMEOUT_ERROR
32784	0x8010	C_CRC_FR1_ERROR
32785	0x8011	R_C_CRC_FR1_ERROR
32800	0x8020	C_R_SEGUE_FRPOWER_ERROR
32801	0x8021	C_R_CRC_FR1_FRPOWER_ERROR
32816	0x8030	FRTRAIN errors placeholder
32832	0x8040	FRSNR errors placeholder
32848	0x8050	C_R_SEGUE_FREXCHANGE_ERROR
32849	0x8051	R_C_SEGUE_FREXCHANGE_ERROR
32850	0x8052	C_R_CRC_FR2_FREXCHANGE_ERROR
32851	0x8053	R_C_CRC_FR2_FREXCHANGE_ERROR
32864	0x8060	C_SEGUE_FRSYNCH_ERROR
32865	0x8061	C_R_SEGUE_FRSYNCH_ERROR
32866	0x8062	R_SEGUE_FRSYNCH_ERROR
32867	0x8063	R_C_SEGUE_FRSYNCH_ERROR
32868	0x8064	R_C_CRC_N_ERROR

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 62 STAT.930 (offset 3)

Bits	Name	Description
3:0	Reserved	
4	Normal/ Standby Status	0 = Modem is in Normal mode (Refer to Bit 4 of OPTN.930) 1 = Modem is in Standby mode (Refer to Bit 4 of OPTN.930)
31:5	Reserved	

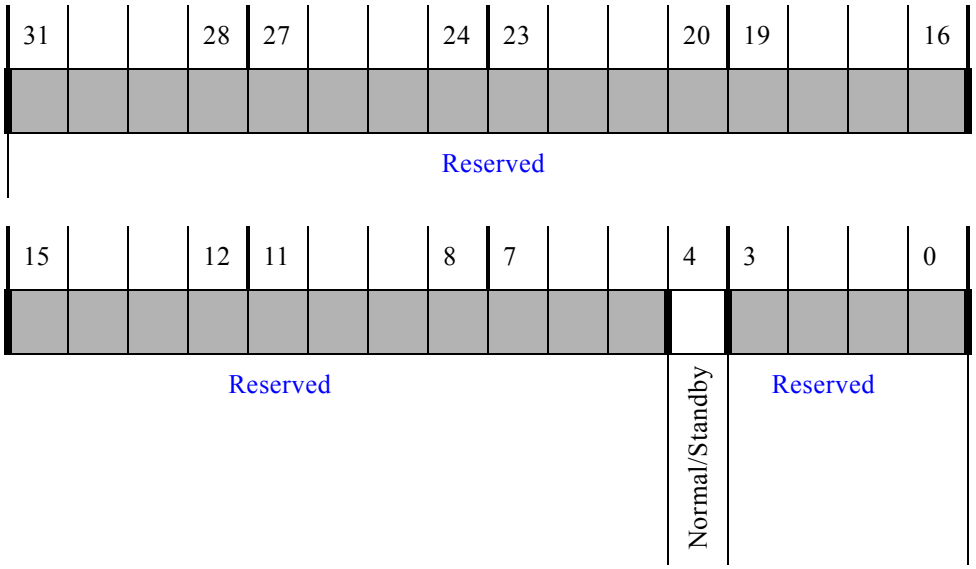


Figure 87. STAT.930 (STAT offset 3)

Table 63 STAT.1pbk_rate (offset 4)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
STAT.1pbk_rate **Description:** This reflects the actual fast and intl latency path rates in the UTOPIA loopback mode. The firmware will override invalid user settings in OPTN. lpbk_rate with valid defaults. (Refer to ANCMV-05)	4	1	ATU-C ATU-R

Bits	Name	Description
7:0		Actual fast path 1pbk data rate
15:8		Actual intl path 1pbk data rate
31:16		Reserved

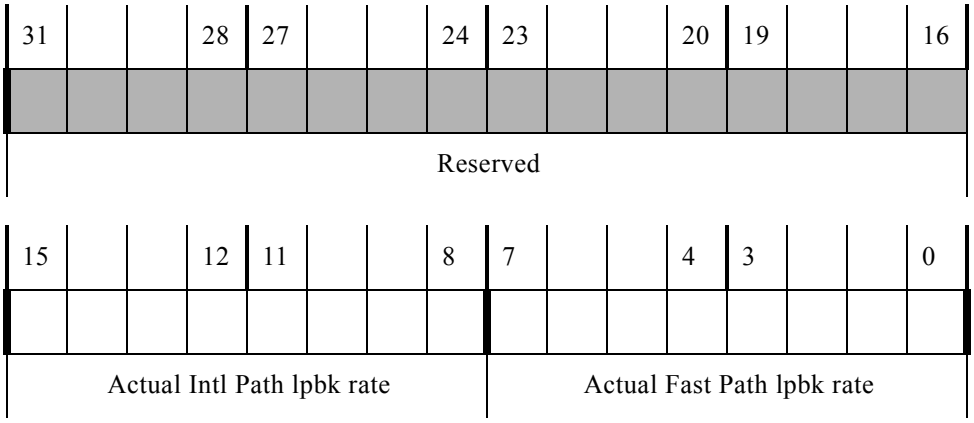


Figure 88. STAT.1pbk_rate (offset 4)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 64 STAT.atm.fifo (offset 5)

(Anaconda/Diamondback/Eagle Specific CMV)

Name	O	L	Access
STAT.atm_fifo **Description:** This reflects the actual Tx and Rx FIFO sizes in each latency path. The firmware will override invalid user settings in OPTN.atm_fifo with valid defaults. (Refer to ANCMV-05)	5	1	ATU-C ATU-R

Bits	Name	Description
4:0		Rx FIFO size Fast Path
12:8		Rx FIFO size Intl Path
20:16		Tx FIFO size Fast Path
28:24		Tx FIFO size Intl Path

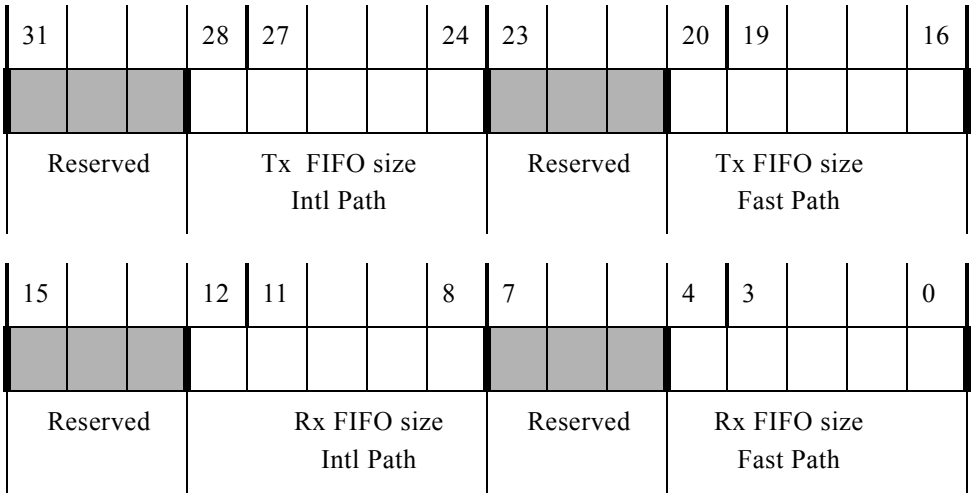


Figure 89. STAT.atm.fifo (offset 5)

Usage

STAT is a read-only CMV requesting the return of a dataword containing the status of the answering ATU. You would use STAT in these different circumstances:

- You want to know what the current state of the ATU is.
- You want to know whether the ATU passed or failed self-tests it undertook when in TEST-HW state.
- You want to know what options are in effect on the upstream and downstream links of an ATU-C.
- You want to know whether the ATU succeeded in initializing links, and, if not, some idea of why.
- You want to know whether certain modem options were in effect, such as Fast Retrain or Lite Mode.
- You want to know whether a profile write succeeded or failed at the hardware level.

Notes

The ATU must be the near end of the ME requesting the tests. Reporting of results from far-end testing is not supported at this time.

Related CMVs

CNTL

Requests a changes of state. Use STAT to find out the results of the request.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

TEST

Summary

Name	O	L	Access	Description
TEST.control	0	1	ATU-C, ATU-R R/W	Starts or stops a test tone on one bin or on all bins at a specified power.
TEST.receive_power	1-31	31	ATU-C R-only	Request return of a dataword containing measured power on one of 30 US bins and 1 DS bin (31).
TEST.receive_power	32-255	224	ATU-R R-only	Request return of a dataword containing measured power on one of 224 DS bins.

Hint: be sure to read the notes.

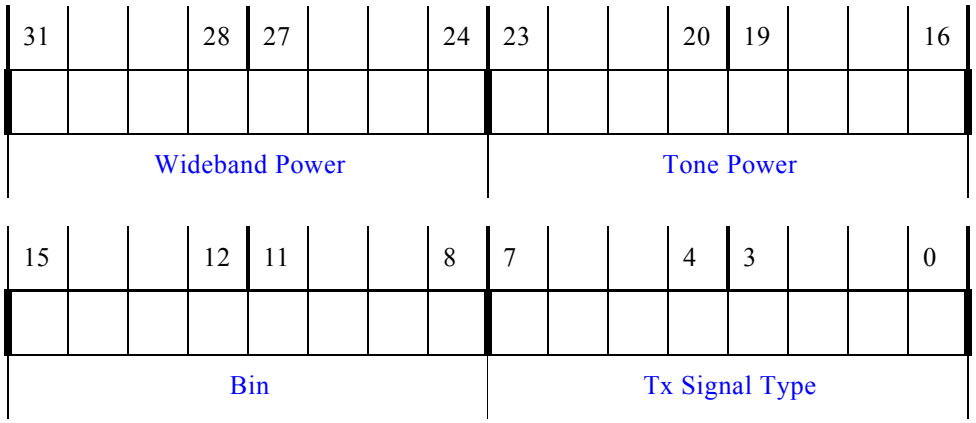


Figure 90. TEST.control (offset 0)

Table 65 TEST.control (offset 0)

Bits	Name	Description
7:0	Tx Signal Type	0x00 Do not send, or stop sending, the test tone. 0x01 Transmit a test tone. 0x02 Transmit a wideband test signal if the ATU is in Full-rate Mode or a reduced wideband test signal if the ATU is in Lite Mode. 0x03 — 0xFF Reserved.
15:8	Bin Field C RT	Specifies the bin on which test tone is to be transmitted. C: 0x00 — 0x1F 0 through 31, one of 31 US and 1 DS bins. RT: 0x20 — 0xFF 32 through 255, one of 224 DS bins.
23:16	Tone Power	Specifies the power, in dBm, that the tone signals are to have. This is a negative integer. The allowed range is -255 dBm to 0 dBm, although signals less than 50 dBm will usually fall below the noise floor. Example: -10 dBm would be represented by 0x0A.
31:24	Wideband Power	Specifies the power, in dBm, that the wideband signal is to have. This is a negative integer. The allowed range is -255 dBm to 0 dBm, although signals less than -50 dBm will usually fall below the noise floor. Examples: 0x1A is -26 dBm 0x20 is -32 dBm

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

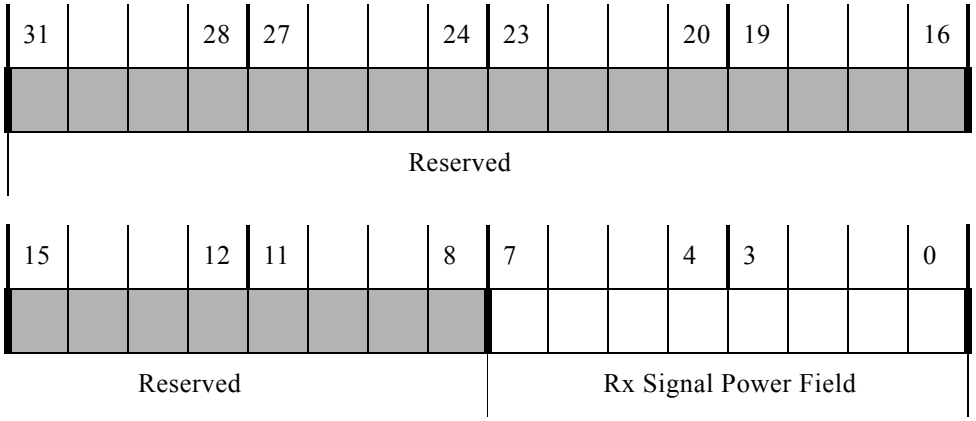


Figure 91. TEST.receive_power (TEST offsets 1-255)

The Rx Signal Power Field (7:0) contains the Rx power being returned.

Usage

The TEST CMV is used to control the transmit signal and measure the received signal at an ATU while it is in TEST-SIGNAL state.

TEST allows you to transmit a test tone of a specified power on a subchannel, or to transmit a wideband signal of a specified power, or to read the power of signals received.

Notes

1. This CMV is only active when the ATU is in one of the TEST states defined in Chapter 2. It will return undefined values otherwise.
2. Notice that there are 30 offsets on the ATU-C TEST.receive_power (Offsets 1-31) but 31 bins. TEST with an offset of 0 would not access bin 0, but would be a TEST.control. However, bin 0 represents the dc bin, which is not used for transmission.
3. Notice that there is an extra ATU-R bin: 225 instead of 224. One of them, however, is used for the pilot tone: bin 64.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Related CMVs

MASK

Enables or disables a set of tones on the bins for ATU training purposes.

TONE

Returns the characteristics of a tone on one bin.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

TONE

Summary

Name	O	L	Access	Description
TONE.upstream	0-30	31	ATU-C R-only	Returns a dataword stating characteristics of the tone on one of the 31 US bins. Offset 0 maps to bin 0, etc.
TONE.downstream	63-287	225	ATU-R R-only	Returns a dataword stating characteristics of the tone on one of the 225 DS bins. Offset 63 maps to bin 31, etc.

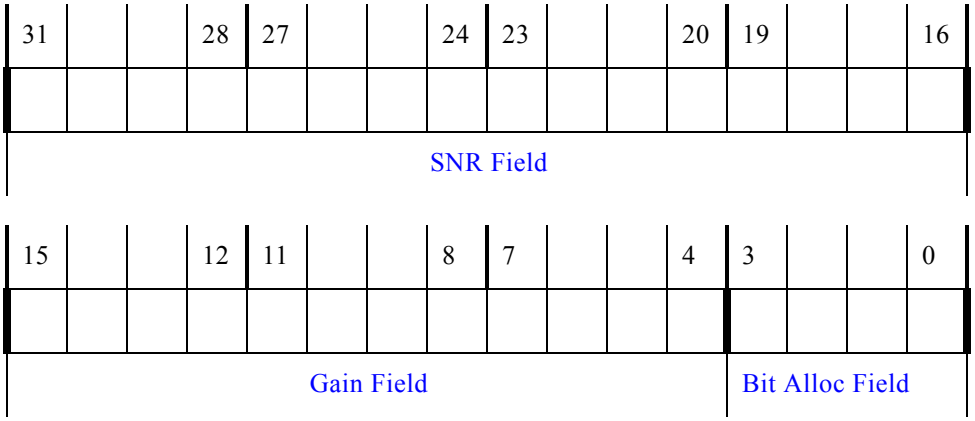


Figure 92. TONE.upstream (TONE offsets 0-30), TONE.downstream (TONE offSET 62-287)

Table 66 TONE.upstream (TONE offset 0-30), TONE.downstream (TONE offset 62-287)

Bits	Field	Value — Hexadecimal
3:0	Bit Alloc	The number of bits per frame currently being transported in the US or DS bin being read.
15:4	Gain	The gain in dB, in 3.9 notation.
31:16	SNR	The measured SNR at the tone frequency, in dB, in 8.8 notation.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Usage

TONE reads SNR, gain, and bit allocation information for each upstream or downstream subchannel. It is updated approximately every 10 seconds.

In both cases, the SNR is given in dB in 8.8 notation, which allows fractional values to be represented by integer variables. In this notation, the most significant eight bits represent the values before the decimal point and the least significant eight bits represent the values after the decimal point.

For example, 0x0100 represents the decimal value 1.0 in 8.8 notation, and 0x0280 represents the decimal value two and eight sixteenths, or 2.5, in 8.8 notation.

Similarly, the gain is given in dB in 3.9 notation, with the most significant three bits representing the values before the decimal point and the least significant nine bits representing the values after the decimal point.

For example, 0x200 represents the decimal value 1.0 in 3.9 notation, and 0x480 represents the decimal value two and four sixteenths, or 2.25, in 3.9 notation.

Notes

1. TONE requires the target ATU to be in OPERATIONAL state. It will return random values otherwise.
2. Upstream SNR information is available at the ATU-C only. Downstream SNR information is available at the ATU-R only.

Related CMVs

MASK

Enables or disables a set of tones on bins for ATU training purposes.

TEST

Places a test tone on a bin and returns the measured power.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

TXDA (Transmit Data)

Summary

Name	O	L	Access	Description
TXDA.data	1-2	2	ATU-C R/W ATU-R R/W	Transmits a message over the EOC to an RXDA.data.
TXDA.Clear_EOC	10	1	ATU-C R/W ATU-R R/W	Receives a message transmitted over the EOC from a TXDA.data.
TXDA.mailbox	11	1	ATU-C R/W ATU-R R/W	Notifies the sender ME that a message is not in TXDA.data.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 67 TXDA.data (offset 1)

Name	O	L	Access
TXDA.data (offset 1) **Description:** Transmits a message over the EOC to a RXDA.data	1	2	ATU-C R/W ATU-R R/W

All 64 bits of TXDA.data (offsets 1 and 2) hold the EOC message.

Bits	Name	Description
31:0	TXDA.data (offset 1)	Actual data to be transmitted

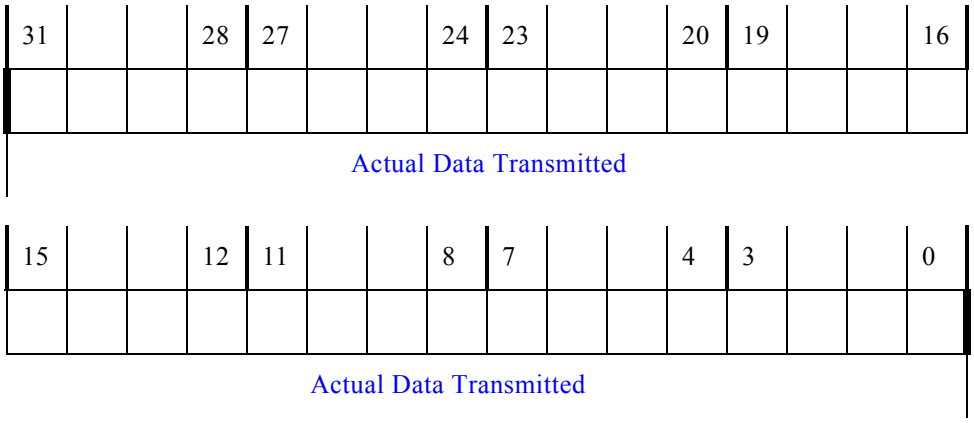


Figure 93. TXDA.data (offset 1)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 68 TXDA.data (offset 2)

Name	O	L	Access
TXDA.data (offset 2) **Description:** Transmits a message over the EOC to a RXDA.data	2	2	ATU-C R/W ATU-R R/W

Bits	Name	Description
31:0	TXDA.data (offset 2)	Actual data to be transmitted

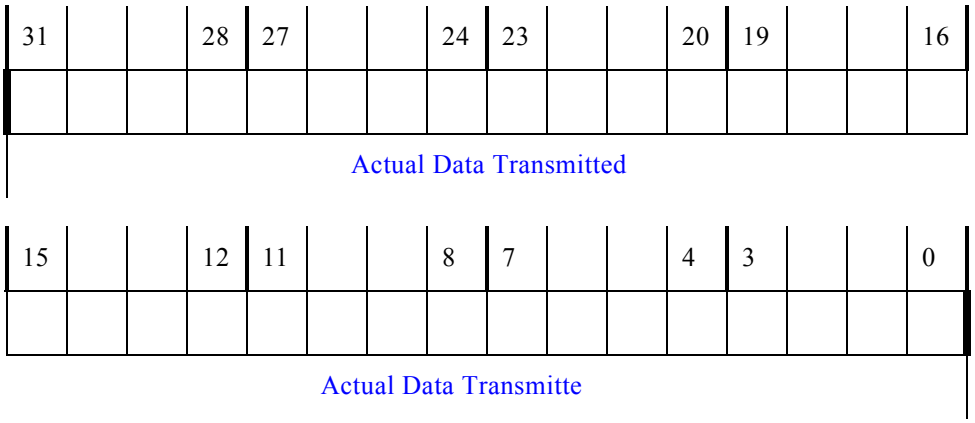


Figure 94. TXDA.data (offset 2)

Table 69 TXDA.Clear_EOC (offset 10)

Name	O	L	Access
TXDA.Clear_EOC (offset 10) **Description:** Transmits a message over the EOC to a RXDA.Clear_EOC	10	1	ATU-C R/W ATU-R R/W

Bits	Name	Description
31:0	TXDA.Clear_EOC (offset 10)	Actual data to be transmitted

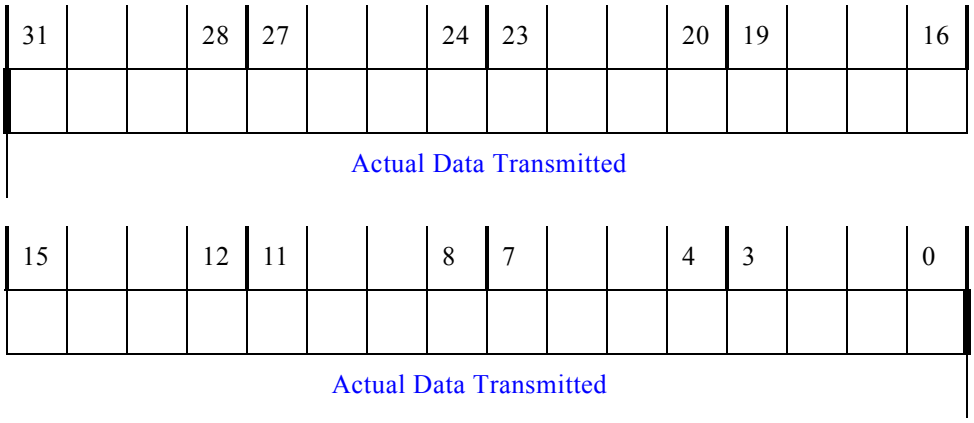


Figure 95. TXDA.Clear_EOC (offset 10)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

Table 70 TXDA.mailbox (offset 11)

Name	O	L	Access
TXDA.mailbox (offset 11) **Description:** Notifies the sender ME that a message is not in TXDA.data	11	1	ATU-C R/W ATU-R R/W

Bits	Name	Description
0	TXDA.mailbox	Notifies the sender ME that a message is not in the TXDA.data.
23:16	Number of bytes received	Displays number of bytes to transmit

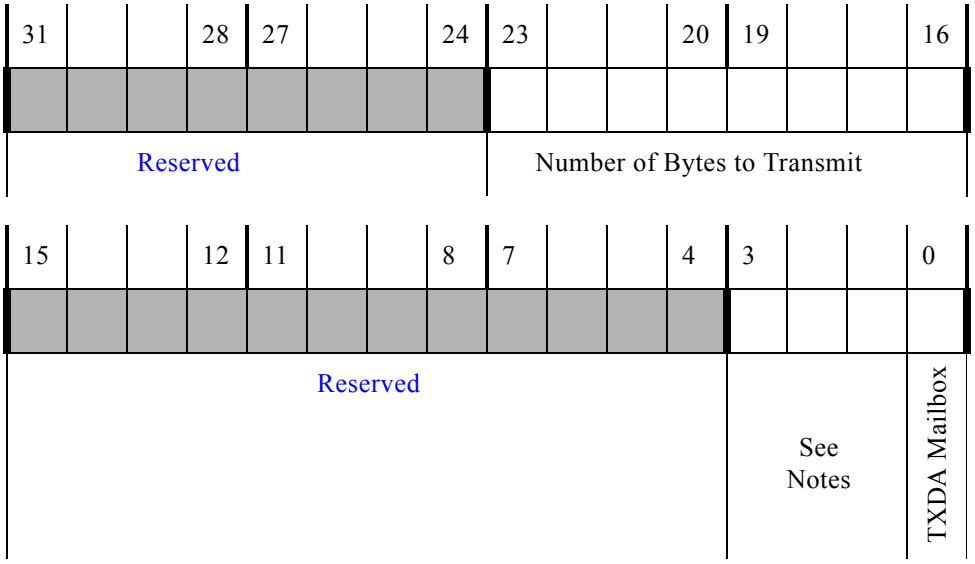


Figure 96. TXDA.mailbox (offset 11)

A set TXDA Mailbox bit means that a message is being transmitted from TXDA.data, and not to write to it.

Usage

Introduction

TXDA can only be used in conjunction with RXDA.

There are two TXDA.data CMVs and two RXDA.data CMVs. A message to be transferred is contained in two 32-bit words; TXDA.data on transmission and RXDA.data on receipt.

Sending a Downstream Message

To send a downstream message,

1. The ME-C checks the ATU-C TXDA Mailbox Bit (TXDA.mailbox, Offset 11, bit 0). If it is set, the ME-C must wait. If it is clear, the ME-C goes on to the next step.
2. The ME-C writes the message data in TXDA.data (TXDA offsets 1-2) at the ATU-C. It need not specify the length of the message.
3. The ME-C begins the transmission by writing a one in the TXDA Mailbox Bit.
4. The ATU-C automatically transmits the data to RXDA.data (RXDA offsets 1-2) of the ATU-R, sets the RXDA Mailbox Bit (RXDA.mailbox, Offset 11, bit 0), and clears the TXDA Mailbox Bit.
5. The ME-R discovers that the message is there. It can do this by polling the ATU-R's RXDA Mailbox Bit, or with a FLAG.mask (FLAG offset 0).
6. The ME-R reads the message and clears the ATU-R's RXDA Mailbox Bit.

Sending an Upstream Message

To send an upstream message,

1. The ME-R checks the ATU-R TXDA Mailbox Bit (TXDA.mailbox, Offset 11, bit 0). If it is set, the ME-R must wait. If it is clear, the ME-R goes on to the next step.
2. The ME-R writes the message data into the TXDA.data TXDA offsets 1-2) at the ATU-R.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

3. The ME-R requests transmission by writing a one in the TXDA Mailbox Bit.
4. The ATU-C continuously polls the TXDA Mailbox Bit at the ATU-R, as long as its own RXDA Mailbox Bit is clear. The ATU-C will not overwrite a message in its own RXDA.data.
5. When the ATU-C finds the ATU-R's TXDA Mailbox Bit set, it reads the ATU-R's TXDA.data into its own RXDA.data.
6. Upon completion, the ATU-C sets its own RXDA Mailbox Bit and the ATU-R clears its own TXDA Mailbox Bit.
7. The ATU-C suspends polling the ATU-R TXDA Mailbox Bit until the ME-C clears the RXDA Mailbox Bit.
8. The ME-C must detect the ATU-C's RXDA.mailbox being set. It can do so by polling or via the Flag Line.
9. On detecting a message, the ME-C reads it.
10. The ME-C clears the ATU-C's mailbox bit.

Note: Please refer to application note ANCMV-04

Notes

The ME can configure the ATU-C and ATU-R to set the PF4 flag when an RXDA Mailbox Bit indicates that a message has been received. See FLAG for a description of this configuration.

A value of **0xF** in TXDA.mailbox causes the ATU-C to retrieve an INFO dataword as well. The ATU-C does not currently retrieve it automatically.

Related CMVs

FLAG

Programs the ATU to trigger the Flag Signal when specified events occur. The Mailbox Bit being set is such an event.

INFO

Returns information identifying the ATU-C or ATU-R. You can use the Mailbox Bit to cause the ATU-C to send one automatically to the ATU-R.

RXDA

Used in conjunction with TXDA.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing.

UOPT (Upstream Options)

Summary

Name	O	L	Access	Description
UOPT.mux_option	0	1	ATU-C R/W	Specifies Interleave Path or Fast Path.
UOPT.simplex_bytes	1	1	Reserved.	
UOPT.duplex_bytes	2	1	ATU-C R/W	Specifies US data rates for 4 options.
UOPT.fast_check_bytes	3	1	ATU-C R/W	Specifies number of fast-path checkbytes for 4 options.
UOPT.intl_check_bytes	4	1	ATU-C R/W	Specifies number of inter-leave-path checkbytes for 4 options.
UOPT.intl_depth	5	1	ATU-C R/W	Specifies interleave depth for 4 options.
UOPT.symbols_per_codeword	6	1	ATU-C R/W	Specifies number of symbols per codeword for 4 options.
UOPT.required_margin	7	1	ATU-C R/W	Specifies the required SNR margin.

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Table 71 UOPT.mux_option (UOPT offset 0)

Bit	Name	Value
4	Mux Option 1	0 Use Fast Path in US for Option 1. 1 Use Interleave Path in US for Option 1.
5	Mux Option 2	0 Use Fast Path in US for Option 2. 1 Use Interleave Path in US for Option 2.
6	Mux Option 3	0 Use Fast Path in US for Option 3. 1 Use Interleave Path in US for Option 3.
7	Mux Option 4	0 Use Fast Path in US for Option 4. 1 Use Interleave Path in US for Option 4.

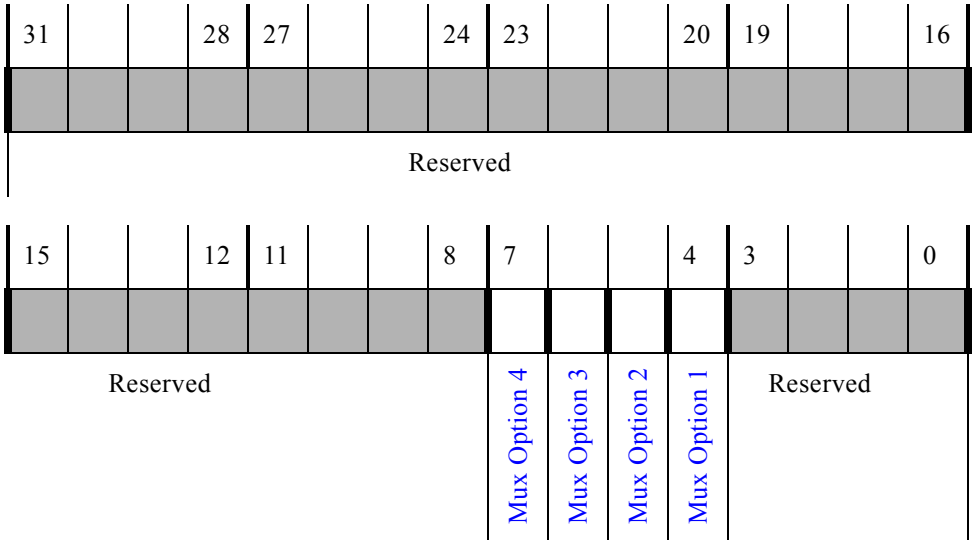

Figure 97. UOPT.mux_option (UOPT offset 0

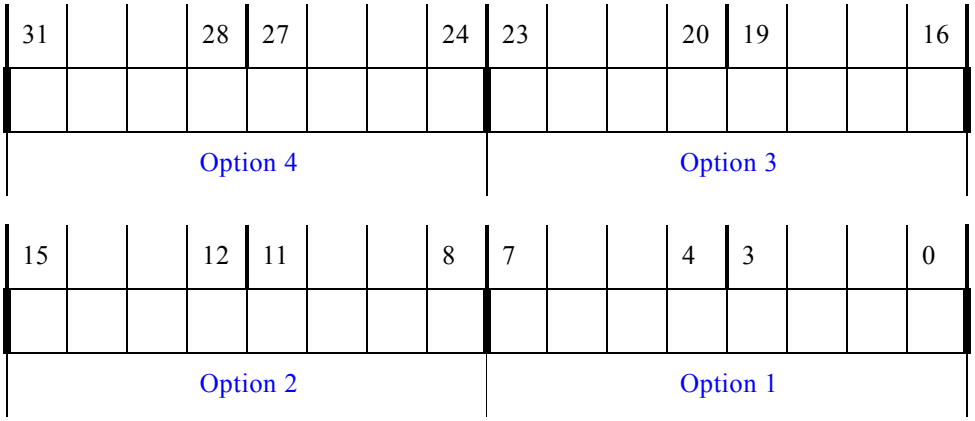

Figure 101. UOPT Offset 2-6

The Option 1, Option 2, etc., Field contains the parameter that is appropriate to that offset for that option. For example, for UOPT.duplex_bytes, the Option 1 Field contains the US data rate to be associated with Option 1, etc.

Table 42 below states the meaning of the option fields for the relevant CMVs.

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Table 72 UOPT Option Field Values

UOPT Name	Option Field Description
UOPT.duplex_bytes (UOPT offset 2)	• Specifies the US data rate in bytes per symbol for 4 options. • The rate in bps is equal to the rate in bytes per symbol multiplied by 32,000. • Rates can range from 0x01 (32 Kbps) to 0xFF (8.16 Mbps) for full-rate, or to 0x30 (1.536 Mbps) for lite. Example: Bytes per symbol = 0x0A. The data rate = 320 Kbps. Example: An US rate of 640 Kbps is required for each option. UOPT data-word value: 0x14141414.
UOPT.fast_check_bytes (UOPT offset 3)	• Specifies the number of checkbytes, in bytes/codeword, on fast-path data. • The values in this word are only valid for Fast Path (UOPT.mux_option) and should be cleared otherwise. • Each possible value must be a multiple of the number of symbols per codeword (UOPT.symbols_per_codeword). • Each value must even and <= 0x14.
UOPT.intl_check_bytes (UOPT offset 4)	• Specifies the number of checkbytes used, in bytes/codeword, on interleave-path data. • The values in this word are only valid for Interleave Path (UOPT.mux_option) and should be cleared otherwise. • Each possible value must be a multiple of the number of symbols per codeword (UOPT.symbols_per_codeword). • Each value must even and <= 0x14.

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Table 72 UOPT Option Field Values

UOPT Name	Option Field Description
UOPT.intl_depth (UOPT offset 5)	• Specifies interleave depth, in bytes (i.e., the number of bytes between previously adjacent bytes after interleaving). • The values in this word are only valid for Interleave Path (UOPT.mux_option) and should be cleared otherwise. • Interleaving is only useful in combination with coding. If you don't select coding, then clear the interleave depth. • The interleave depth must be a power of 2 and < 64. • The expression **(interleave depth * symbols/codeword) > 255** must be true.
UOPT.symbols_per_codeword (UOPT offset 6)	• Specifies the codeword length, in symbols per codeword, for 4 options. • The multiple-frame-per-codeword feature is only available for Interleave Path. The value must be 1 for Fast Path. • The value must be a power of 2, up to a maximum of 64. • The expression **(Data Bytes + Overhead/Symbol)*** **(Symbols/codeword + Parity Bytes) <= 255** must be true, where the Overhead/Symbol is determined by the framing mode selected, as defined in *[1]*.

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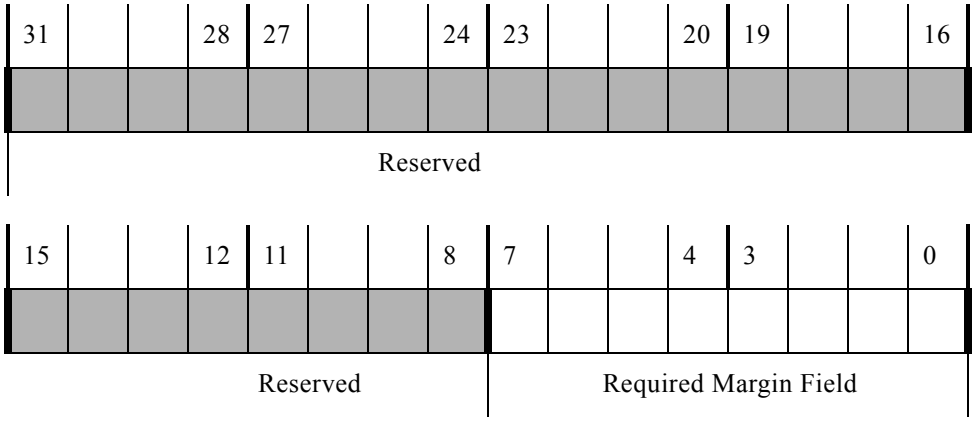
Figure 102. UOPT.required_margin (offset 7).



This CMV allows you to specify the required upstream SNR margin, in dB. It is the same for all four options.

For example, if you set this parameter is to 6, the AD20MSP918 will require the link to maintain a link margin of 6 dB, based on a target bit error rate (BER) of 1.0E-7. If this margin is not met, the link initiation will fail.

The nominal value for the required margin is 6dB. This margin does not include coding gain.

The margin must be less than 127 (decimal).

Usage

UOPT sends US configuration parameters for four options to the ATU-C. DOPT (for downstream parameters) and UOPT are only used when you select Explicit-rate Configuration option in the Configuration Control field of CNTL.control (Offset 0). If the ME does not properly and completely set DOPT and UOPT, the results of the initialization will be undefined.

DOPTs and UOPTs are basically of two types: interleave-path and fast-path. The field values support one of these concepts or the other.

Interleaving is used to spread out burst errors prior to the error correction stage. The purpose is to reduce the number of errors seen within any one Reed-Solomon codeword.

Recall that the number of errors within each codeword that can be corrected is equal to half the number of parity bytes. As the interleave depth is increased, burst errors become more spread out and the Reed-Solomon effectiveness increases. The cost is an increase in latency.

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Increasing the frames per codeword allows lower data rates to operate with larger codeword sizes and better performance.

Notes

None.

Related CMVs

DOPT

Specifies the DS configuration parameters.

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Application Notes

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ANCMV-01

New Margin/Latency Interface

Release 3.1 contains an improved interface for the CO to specify a target margin (ex: 6dB) and a maximum latency requirement (e.g. 0.25 ms) for the upstream and downstream. Specifically, the ME now only needs to specify the target margin and maximum latency and the chipset automatically calculates the optimum coding (Interleaving, Reed-Solomon and TCM, if enabled), calculates the gain due to that coding, and calculates the achievable data rate. This eliminates the need for the ME to do any of these calculations.

In previous releases of 930 code Rate Adaptive Links could only be configured using CMVs ADPT 0 & 1 (RA1) for Downstream (DS) and Upstream (US) respectively. The method of Margin selection using these CMVs requires that the ME assume that the chipset will provide a fixed margin improvement due to coding gain. Unfortunately, the amount of margin improvement varies based on link conditions and the coding parameters chosen by the chipset for those conditions. ADI has provided guidelines for setting up the desired margin field in the ADPT CMV, but it was found that in some cases the Noise Margin obtained was not uniform. The Chipset performed as expected on ANSI Loop tests with noise in the Downstream, and was conservative in the Upstream. When Noise tests were conducted on Loopreach, the DS Noise Performance varied from Conservative on Shorter loops to Aggressive on Longer loops, while US Noise Performance continued to be Conservative across all loops. Some changes were made that improved the Margin Performance of the original Rate Adaptive Interface (ADPT 0 & 1) with version 3.1, making it more consistent across Loopreach.

In an attempt to improve the situation while also maintaining backward compatibility, ADI has created a new Rate Adaptive Interface (RA2) using ADPT 4 & 5 for configuring Downstream and ADPT 6 & 7 for configuring Upstream. The RA1 CMVs ADPT 0 & 1 still exist and can be used for initiating a Rate Adaptive Link with performance similar to earlier releases. With ADPT 4-7 the ME configures the Desired Margin, Max Interleave Depth, Max Symbols/Codeword and Maximum Latency. Then the optimum coding, interleave depth and Symbols /Codeword are automatically determined to achieve the desired performance margin while maintaining target Latency requirement. ADPT 4 & 6 are also used for setting the Max and Min Data Rates, selecting a Data Path and for determining whether or not Coding should be enabled. To use the New Rate Adaptive User Interface, simply set ADPT 5 bit 31.

With FW ver 3130be51, if the user-enabled RA2 and the CPE was v2.2 or earlier, the interface would automatically switch over to using RA1. Unfortunately, this required that the user populate the RA1 parameters, as none of the settings selected by the user were transferred over. With the v3.1 patch, if the user enables RA2, the RA2 will be used to generate DS options, eliminating this problem. If the v3.1 patch links to any CPE with a FW ver older than v3.1 patch (including v3.1), it will not attempt to figure out coding gain. Basically, it will take the Bmax from R-MSG-RA, convert it to payload and generate options from this value. It essentially generates options similar to how RA1 generates options; however, it will restrict Latency, Intl Depth, etc. as specified by the user.

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Original ADPT CMV (RA1) offsets 0 to 1 (ATU-C only)

ADPT.downstream (Offset 0) (default = 0x33FF0001)

Bits 8:0	DS min rate	(default = 0x01)
Bits 15:9	Interleave Depth	(default = 0x00)
Bits 24:16	DS max rate	(default = 0x1FF)
Bit 25	DS coding enable	(1-on (default), 0-off)
Bit 26	Path Type	(0-intl (default), 1-fast)
Bit 27	RESERVED	(default = 0)
Bits 31:28	DS Required Margin	(default = 3)

ADPT.upstream (Offset 1) (default = 0x60FF0001)

Bits 8:0	US min rate	(default = 0x01)
Bits 15:9	Interleave Depth	(default = 0x00)
Bits 24:16	US max rate	(default = 0xFF)
Bit 25	US coding enable	(1-on, 0-off (default))
Bit 26	Path Type	(0-intl (default), 1-fast)
Bit 27	RESERVED	(default = 0)
Bits 31:28	US Required Margin	(default = 6)

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New ADPT CMV (RA2) offsets 4 to 7 (ATU-C only)

ADPT.ds_config (Offset 4)(default = 0x63FF0001)

Bits 8:0	DS min rate	(default = 0x01)
Bits 15:9	RESERVED	(default = 0x00)
Bits 24:16	DS max rate	(default = 0x1FF)
Bit 25	DS coding enable	(1-on (default), 0-off)
Bit 26	Path Type	(0-intl (default), 1-fast)
Bit 27	RESERVED	(default = 0)
Bits 31:28	DS Required Margin	(default = 6)

ADPT.ds_latency (Offset 5) (default = 0x00407F7F)

Bits 6:0	Max DS latency, 0.25ms steps	(default = 0x7F)
Bits 7	RESERVED	(default = 0)
Bits 14:8	Max DS symbols/codeword (Smax)	(default = 0x7F)
Bit 15	RESERVED	(default = 0)
Bits 22:16	Max DS interleaver depth (Dmax)	(default = 0x40)
Bits 30:23	RESERVED	(default = 0)
Bit 31	Enable new ADPT CMV i/f (US & DS)	(0-off (default), 1-on)

ADPT.us_config (Offset 6) (default = 0x63FF0001)

Bits 8:0	US min rate	(default = 0x01)
Bits 15:9	RESERVED	(default = 0x00)
Bits 24:16	US max rate	(default = 0x1FF)
Bit 25	US coding enable	(1-on (default), 0-off)
Bit 26	Path Type	(0-intl (default), 1-fast)
Bit 27	RESERVED	(default = 0)
Bits 31:28	US Required Margin	(default = 6)

ADPT.us_latency (Offset 7) (default = 0x00407F7F)

Bits 6:0	Max US latency, 0.25ms steps	(default = 0x7F)

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Bits 7	RESERVED	(default = 0)
Bits 14:8	Max US symbols/codeword (Smax)	(default = 0x7F)
Bit 15	RESERVED	(default = 0)
Bits 22:16	Max US interleaver depth (Dmax)	(default = 0x40)
Bits 31:23	RESERVED	(default = 0)

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ANCMV-02

CODING GAIN, MARGIN, AND ERROR PERFORMANCE

In digital communication systems, error-control coding is often applied to provide better error performance for a given data rate, at the expense of increased bandwidth, aggregate data rate, and system complexity. The various ADSL standards allow use of specific error correction codes, called Reed-Solomon codes, to implement this feature on standard compliant ADSL systems. This coding technique is employed on the Analog Devices family of ADSL chipsets. The error correction capability of these coding techniques allows a communication system to transmit data at a higher rate; this higher rate incurs a higher number of channel errors, but, if properly chosen, the error correction code will reduce the payload error rate down to desired values.

Effective coding reduces the margin required to provide a desired link quality, as measured by payload error rate. For example, if a link must operate with 6 dB noise margin to provide a given error quality without coding, it may be possible to apply coding and operate at a 1 dB noise margin if optimal coding is applied. Operation at this lower noise margin will in most cases, allow operation at a higher data rate while providing the same error performance. This difference in margin requirements with and without coding is often called "coding gain," which is used as a figure of merit for effectiveness of coding. In the example above, the coding gain is 6 - 1= 5 dB.

Trellis coding, when enabled, will also provide a small coding gain that affects the relationship between the SNR noise margin required during link initiation and the ultimate performance margin and error performance of that link.

In ADI code releases prior to Release 3.1, the Management Entity was required to account for coding gain when setting the link margin for a given link. In general, the Management Entity would require that the link maintain a given noise margin (not including the effects of coding gain) when determining the allowable data rate during ADSL link initiation. The burden was on the Management Entity to account for coding gain in the "desired margin" setting prior to link initiation to get the best combination of error performance vs. data rate. In the example above, if the Management Entity was attempting to link at a final performance noise margin of 6 dB, it would need to program the ADI chipset to use an SNR margin of 1 dB during link initiation. The coding gain of 5 dB would increase the SNR margin of 1 dB to the desired performance margin of 6 dB, with the associated error performance.

Unfortunately, the precise calculation of coding gain in a DMT ADSL system is very complex. Coding gain can vary based on a number of factors; data rate, parity bytes, and interleave depth (related to latency) are all factors which can affect the coding gain. Because, in a typical rate adaptive ADSL link, the Management Entity has limited knowledge of many of these parameters, it has been cumbersome for the ME to calculate coding gain for all conditions. As a result the Management Entity may not always set the SNR

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margin for a given link optimally; typically the Management Entity uses a conservative link initiation margin in order to provide the required error performance over a wide range of loops. Use of such a conservative margin may sacrifice data rate on some loops.

In Release 3.1, ADI is providing a "performance margin interface." When this margin interface is used, the Management Entity provides the target margin (i.e., the ultimate margin desired, corresponding to the desired error performance-6 dB in the example above) and the chipset calculates the optimal data rate for that desired margin, including the effects of coding gain. The chipset calculates coding gain based on the data rate and other parameters negotiated during link initiation. The coding gain calculation used by the chipset is based on extensive simulations and experimental testing and is therefore usually more accurate than estimates used by the Management Entity in previous ADI releases.

This new interface simplifies the margin selection prior to link initiation and allows users to more easily and accurately get the maximum data rate for a given error performance. However, we recognize that several ADI customers have significant operational experience in using link initiation margin that does not account for coding gain, as in previous firmware releases. We further recognize that these customers may want to continue to utilize their own empirical experience as a guideline for future operation. Specifically, we expect that some customers who currently use the older link initiation SNR margin scheme may desire a mapping of the old SNR link initiation margin to the new performance margin.

MAPPING OF OLD MARGIN REQUIREMENT TO NEW MARGIN REQUIREMENT

Fundamentally, the difference between the link initiation SNR margin used in older releases and the corresponding performance margin used in Release 3.1 is the coding gain. As mentioned above, the coding gain calculation is quite complex, so an exact mapping of SNR link initiation margin to performance margin is unrealistic. Fortunately, by using a few simple "rules of thumb" a reasonably accurate coding gain calculation can be provided that will be accurate for most link conditions.

CODING GAIN CALCULATION-UPSTREAM

1. Whenever Reed-Solomon FEC coding is used, assume a flat coding gain of 4 dB.

2. Add an additional 1 dB if the interleave depth is 4 or higher.

3. If trellis coding is used, add an additional 2 dB of coding gain if the interleave depth is 4 or higher.

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NOTES:

a) Trellis coding is not available on some CPE. When linking with a CPE that does not support trellis coding, the ADI chipset will not use trellis coding, even if requested by the operator during setup.

b) Trellis coding was not supported on earlier ADI firmware releases.

EXAMPLE

Assume a link with maximum interleave depth and no trellis coding, and assume that the link initiation SNR margin has been set to 2 dB. The coding gain will be 4 dB from the Reed-Solomon coding, plus an additional 1 dB for using interleaving, for a total coding gain of 5 dB. To achieve the same error performance using the new performance margin interface, the user should ask for 2 + 5 = 7 dB.

CODING GAIN CALCULATION-DOWNSTREAM

1. Whenever Reed Solomon FEC coding is used, assume a flat coding gain of 5 dB.

2. Add an additional 1 dB if the interleave depth is 4 or higher.

3. If trellis coding is used, add an additional 2 dB of coding gain if the interleave depth is 4 or higher. NOTES:

a) Trellis coding is not available on some CPE. When linking with a CPE that does not support trellis coding, the ADI chipset will not use trellis coding, even if requested by the operator during setup.

b) Trellis coding was not supported on earlier ADI firmware releases.

EXAMPLE:

Assume a link with zero interleave depth and no trellis coding, and assume that the link initiation SNR margin has been set to 2 dB. The coding gain will be 5 dB from the Reed Solomon coding, and there will be no additional coding gain due to interleaving or trellis coding, so the total coding gain is 5 dB. To achieve the same error performance using the new performance margin interface, the user should ask for 2 + 5 = 7 dB.

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ANCMV-03

Analog Loopback

An analog loopback self-test capability has been added to the Anaconda chipset. This feature is meant for verifying basic analog integrity of an ADSL port for manufacturing and debugging purposes. The port under test generates a tone on bin33 (POTS) or bin65 (ISDN) with a fixed power. Power from this tone is reflected by the hybrid back to the receiver of the port under test. The self-test code compares the receive power to a threshold level for proper operation and generates a pass/fail indicator based on the received power level

NOTE: The hybrid will only reflect power at a known level if the port under test. For this reason, it is extremely important that no device is connected to the port under test when performing the analog loopback self-test. If a device is connected to the port under test, false failure indications may result.

This test can be enabled only when the port under test is in "TEST" state. Specifically, the test must be performed using the following steps (note, all CMV settings are for the port under test):

1. Set the CNTL 0 CMV to 0 (reset the port under test)
2. Set the CNTL 0 CMV to 4 (go to TEST state)
3. Read the STAT 0 CMV. It should return the value 0x400, indicating that the port is now in TEST state
4. Set the TEST 0 CMV to 0xF2101 (0xF4101 for Annex B). This commands the modem to output a tone on bin 33 (bin 65 for Annex B) at the proper power level for this test.
5. Read the STAT 0 CMV. A value of 0x20400 indicates that the test has successfully passed. A value of 0x400 indicates that the test has failed.

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ANCMV-04

1) To enable Clear EOC set OPTN 4 bit 15.

2) If Clear EOC is operational stat 0 bit 16 will automatically be set.

3) The CMV's needed to transmit and receive data over the Clear EOC are:

a) TXDA 10 bits (31:0) - actual data to be transmitted
[Byte4;Byte3;Byte2'Byte1], Byte 1 is the MS Byte, sent first

b) TXDA 11 bits (23:16) - number of bytes to transmit

c) RXDA 10 bits (31:0) - actual data received
[Byte4;Byte3;Byte2'Byte1], Byte 1 is the MS Byte

d) RXDA 11 bits (23:16) - number of bytes received

4) Only four bytes can be sent or read at one time via TXDA 10 and RXDA 10.

a) To send data, first write the byte information into TXDA 10. Then write the number of bytes to TXDA 11 (23:16). (Up to four bytes)

b) If it is necessary to send more than 4 bytes, repeat step a) above.

c) The firmware poles TXDA 11 (23:16). Once the byte count is greater than zero, the data will be transmitted.

d) Once data is transmitted, TXDA 10 and TXDA 11 (23:16) are automatically reset. At this point additional data can be sent using TXDA 10 and TXDA 11 (23:16).

e) If the byte count in RXDA 11 (23:16) is 0 the firmware will automatically check the receive buffer for data.

f) If there is data in the buffer, but on the previous check the buffer was empty, RXDA 11 will be updated with a byte count of one. Subsequent reads will register byte counts of up to four as long as the internal Rx buffers contains data.

g) RXDA 11 (23:16) must be set back to zero after reading RXDA 10 each time.

5) See Example below

a) In this example, the number of bytes being sent is known, but this is usually not the case. The general rule for receiving data is loop through:

i) Check byte count (RXDA 11 (23:16))
ii) If non-zero, read that many bytes from RXDA 10
iii) Process read data as desired
iv) Reset RXDA 11 (23:16).

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Example:

To send 4 bytes upstream

//set CO and RT cmv's as desired, be sure to set OPTN 4 bit 15 //then initiate link

//select RT //if no data is currently being sent, write data to TXDA 10 *cr TXDA 11*
st txda11 *Math txda11 = txda11 & 0x00FF0000* *if (txda11 == 0) cw TXDA 10 0x11223344*

//set TXDA 11 to number of bytes to be sent *cr TXDA 11* *st txda11*
MAth txda11 = txda11 & 0xFF00FFFF *MAth txda11 = txda11 | 0x00040000* *cw TXDA 11 txda11*

//select CO, if testing in WINHOST pause 3 seconds //check byte count, if not zero read RXDA 10 *cr RXDA 11* //since this is the first read after an empty buffer, the count will be one
st rxda11 *MAth rxda11 = rxda11 & 0x00FF0000*

if (rxda11 > 0)

{

cr RXDA 10 //0x00000044
st rxda10_read1

}

//clear the counter **!!!!!!!!!!!!!!VERY IMPORANT!!!!!!!!!!!!!!!!!**

cr RXDA 11 *sto temp*
MAth temp = temp & 0xff00ffff *cw RXDA 11 temp* //if in WINHOST pause 3 seconds

//check byte count, if not zero read RXDA 10 *cr RXDA 11*
//maximum count 4, (3 in this case) *st rxda11*
MAth rxda11 = rxda11 & 0x00FF0000 *if (rxda11 > 0)* {
cr RXDA 10 //0x00112233
st rxda10_read2 }

//clear the counter **!!!!!!!!!!!!!!VERY IMPORANT!!!!!!!!!!!!!!!!!**

cr RXDA 11
MAth temp = temp & 0xff00ffff
11 temp
3 seconds

sto temp
cw RXDA
//if in WINHOST pause

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ANCMV-05

ATM/UTOPIA Loopback Mode

Overview

The Anaconda UTOPIA loopback test mode supports Level 2 UTOPIA operation via Port A and Port B of the UTOPIA interface. It also supports both single and dual latency.

To place an Anaconda port in loopback mode, the ME transitions it to the TEST-LOOP-BACK state using the CNTL offset 0 CMV. The entry of the modem into this state is reflected in the 'SW-Status' field of the STAT offset 0 CMV. The ATU remains in the TEST-LOOPBACK state until reset by the ME.

In loopback mode, the Anaconda accepts ATM cells over the UTOPIA interface from an end device and performs the correct ADSL framing operations just as it would on a regular link, then transmits it to be processed further as ADSL data. The framed TX data is then transmitted but is ahead of being fed into the Tx DMT engine, it is looped back internally to the receiver. The Rx decoder knows no better than to treat this incoming data as it would on a regular link, as if it came from the Rx DMT engine. The Rx decoder performs the correct receive framing operations and passes the ATM cells back to the end device in the UTOPIA interface.

The chipset has no built-in mechanism for comparing transmitted cells to received cells. For this reason, the chipset does not determine whether a loopback test passes or fails. Instead, the comparison of transmitted cells to received cells and the associated pass/fail decision must be implemented externally to the chipset.

Features

Prior to entering the loopback test mode, the ME can configure its operation using the following OPTN CMV offsets:

- OPTN.lpbk_config (OPTN offset 13)
- OPTN.lpbk_rate (OPTN offset 14)
- OPTN.atm_fifo (OPTN offset 15)

The firmware accepts the CMV input from the ME and maps it to the relevant Anaconda registers settings.

Some features of the Anaconda configuration in the UTOPIA loopback testmode are fixed and not configurable by the ME. These are as follows:

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- ADSL Framing Mode 2 only
- RS (Reed Solomon) coding not available
- S is fixed at 1 symbol per codeword
- ATM mode only (STM not supported)

Other features of the Stryfe-B DTIR setup in the UTOPIA loopback test mode are configurable by the ME. These are as follows:

- Configurable for Level 1 or Level 2 UTOPIA operation. Note: Level 1 supports single latency only i.e. Intl or Fast path but not both. Level 2 supports dual latency i.e Intl or Fast path or both.
- Configurable data rates for Fast path and/or Intl path.

The following limitations apply to user data rate selections. If single latency:

- Max Intl payload = 253 bytes (allows for 2 bytes of overhead associated with FM 2)
- Max Fast payload = 253 bytes (allows for 2 bytes of overhead associated with FM 2)

If dual latency:

*Max of "Intl + Fast" = 360 bytes

- Configurable for Cell mode and Octet Tx modes
- Configurable Tx and Rx UTOPIA addresses for Fast and Intl path
- Configurable ATM Tx and Rx FIFO sizes
- Configurable ATM scrambling, on or off
- Configurable ADSL scrambling, on or off

CMVs for ATM loopback configurations

OPTN.lpbk_cfg (OPTN CMV with offset 13)

Set up general loopback features. Default value is **0x00000102**

7:0 Fast path ATM address (default is 2, same value used for Tx and Rx address, unused in UTOPIA Level 1 mode).

15:8 Intl path ATM address (default is 1, same value used for Tx and Rx address, unused in UTOPIA Level 1 mode).

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16 if '0', Interleaver off (default);
if '1', interleaver on and interleaver depth is '8'.

20 if '0', UTOPIA Level 1 (default);
if '1', UTOPIA Level 2.

21 if '0', cell Tx mode (default, always cell mode in UTOPIA Level 2);
if '1', octet Tx mode (only valid in UTOPIA Level 1 mode);

24 if '0', ADSL scrambling on (default);
if '1', ADSL scrambling off.

25 if '0', ATM scrambling on (default);
if '1', ATM scrambling off.

OPTN.lpbk_rate (OPTN CMV with offset 14)

Set up Fast and Intl path data rate. Default value is **0x0000B400**.

7:0 Fast path data rate (defaults to 0).

15:8 Intl path data rate (defaults to 0xB4, 180 decimal).

For single latency:

Max Intl payload = 253; if greater than 253, then max value is set.
Max Fast payload = 253; if greater than 253, then max value is set.

For dual latency:

Max allowed value of "Intl+Fast" = 360; if greater than 360 then both Intl and Fast payload is assigned to 0xB4 (180 decimal).

OPTN.atm_fifo_new (OPTN CMV with offset 15)

This sets up the Tx and Rx FIFO sizes in each latency path. Default value is **0x02020202** (See application-notes section of Multiport Users Manual)

STAT.lpbk_rate (STAT offset 4)

OPTN.lpbk_rate reflects what the user has selected with respect to required fast path and intl path data rates. However, the user section can be overridden by the firmware as a result of applying the specified limits. STAT offset 6 reflects the actual Fast and intl path data rates applied in the ATM/UTOPIA loopback mode.

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STAT.atm_fifo (STAT CMV with offset 5)

This reflects the actual Tx and Rx FIFO sizes in each latency path. The firmware will override invalid user settings in OPTN.atm_fifo with valid defaults. (application-notes section of Multiport Users Manual)

Examples of OPTN.lpbk_rate and STAT.lpbk_rate settings

OPTN.lpbk_rate reflects what the user has selected with respect to required data rates in the Intl and Fast latency paths. Since the data selected by the user can be overridden by the firmware as a result of applying the specified limits, STAT offset 4 reflects the actual data rates applied on each latency path.

INTL CMV

The INTL reports the interleaver depth on the US and DS data paths.

Alarms, QoS Indicators, and Counters in the DIAG CMV

The ADSL Multiport chipset automatically gathers performance data and statistics without requiring configuration from the ME. The resulting information available to the ME is a superset of that required by T1.413. Both the near-end and far-end diagnostics information can be read at the ATU-C. Only the near-end diagnostic information can be read at the ATU-R

NOTE: ATU-R performance information is maintained independently at the ATU-R (as near-end information) and at the ATU-C (as far-end information).

The near-end information is based on local indicator bits and other local measurements and observations, while the far end information is calculated based on indicator bits sent from the ATU-R to the ATU-C, as described in the T1.413 standard. Because indicator bits messages can be lost or corrupted, there can be discrepancies between the far-end information at the ATU-C and the near-end information at the ATU-R during normal operation.

DIAG flags

DIAG.flags provide access to the indicator bits and the failures derived from the indicator bit information. These bits are set and cleared automatically as defined in the T1.413 Standard.

DIAG.flags_latched is set in an identical manner to their unlatched counterparts. However, these flags must be explicitly cleared in one of two ways. The latched registers can be explicitly cleared using the DIAG.control CMV, as discussed above. The latched registers will also be automatically cleared whenever they are read; this functionality will avoid race conditions that can occur if separate read and clear commands are used.

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The DIAG CMV also provides total near-end and far-end errored second counts.

DIAG Control

Information in the DIAG.flag_latched CMV is cleared automatically when read. Alternatively, the DIAG.control CMV can be used to clear latched flags as well as diagnostics counts. Note that the DIAG.control CMV can also be used to perform other simple diagnostic functions.

When the ME requests that the ATU-C clear the far-end counts, only the far-end information stored locally at the ATU-C is cleared. The corresponding near-end information at the ATU-R is not cleared; it can only be cleared locally by the ME-R using the DIAG.control CMV. The DIAG.control CMV can also be used at the ATU-C to request corrupt CRCs on the upstream and downstream paths. The DIAG.control register is read/write-only.

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Document History

Revision	Date	Summary	Editor	Tech Writer
1.0	12-3-01	Complete rewrite	Dick Fortin	Tom Quinlan
1.0	12-6-01	Added Mask offset 9	Dick Fortin	Tom Quinlan
1.0	1-14-02	Reformated bit maps	Dick Fortin	Tom Quinlan
1.0	1-22-02	Edited INFO Section	Dick Fortin	Tom Quinlan

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